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Analytical Comparison between Capacitor Assisted and Diode Assisted Cascaded Quasi-Z-Source Inverters

Abstract. *The quasi-Z-source inverter is a very attractive topology because of its unique capability of voltage boost and buck functions in a single stage. But its voltage boost property could be a limiting feature in some applications where very high input voltage gain is required. The input voltage gain could be extended by the implementation of the cascaded quasi-impedance network. This paper discusses four novel cascaded quasi-Z-source inverters. Steady state analysis of topologies operating in continuous conduction mode is presented. Performances of topologies were compared and experimentally validated. Moreover, some problematic issues of proposed topologies were pointed out and discussed.*

Streszczenie. *Quasi-Z falownik z prostym obwodem impedancyjnym jest bardzo interesującym rozwiązaniem topologicznym ze względu na unikalną możliwość jednostopniowego przekształcanie DC/AC w połączeniu z funkcjami obniżania i podwyższania napięcia. W niektórych aplikacjach jego właściwości podwyższające są jednak niewystarczające. Wyższe napięcie wejściowe można uzyskać w wyniku zastosowania w quasi-Z-falownikach kaskadowych obwodów impedancyjnych. W artykule omówiono cztery nowe topologie kaskadowych quasi-Z-falowników. Przedstawiono wyniki analizy stanów statycznych tych układów przy przewodzeniu ciągłym. Porównano właściwości badanych topologii, zweryfikowane eksperymentalnie. Omówiono także inne problemy związane z proponowanymi układami. (**Porównanie analityczne układów kaskadowych quasi-Z-falowników z kondensatorem wspomagającym i z diodą wspomagającą**).*

Keywords: quasi-Z-source inverter (qZSI), PWM converter, continuous conduction mode (CCM), discontinuous conduction mode (DCM).
Słowa kluczowe: quasi-Z-falownik, przekształtnik PWM, tryb przewodzenia ciągłego, tryb przewodzenia impulsowego

Introduction

Quasi-Z-source inverter (qZSI) is a new promising power conversion technology perfectly suitable for interfacing of renewable (i.e., photovoltaic, wind turbines) and alternative (i.e., fuel cells) energy sources [1-3]. The qZSI has the following advantages:

- boost-buck function by the one-stage conversion;
- continuous input current (input current never drops to zero, thus featuring the reduced stress of the input voltage source, which is especially topical in such demanding applications as power conditioners for fuel cells and solar panels);
- excellent reliability due to the shoot-through withstanding capability;
- low or no in-rush current during start up;
- low common-mode noise.

However, the efficiency and voltage gain of the qZSI are limited and comparable with the conventional system of a voltage source inverter with the auxiliary step-up DC/DC converter in the input stage [4]. The concept of extending the qZSI gain without increasing the number of active switches was recently proposed by several authors [5-8]. These new converter topologies are commonly referred to as the *cascaded qZSI* or *extended boost qZSI* and could be generally classified as capacitor assisted (CA) and diode assisted (DA) topologies [5]. In this paper four different cascaded qZSIs with continuous input current will be presented, analyzed and compared. Moreover, some problematic issues of these converters will be pointed out and discussed.

Cascaded qZSIs – Basic Topologies

It should be noted here that this paper provides a general coverage of the cascaded voltage-fed qZSIs with continuous input current. All the topologies to be discussed and analyzed have a common property - the input inductor L_1 that buffers the source current. It means that during the continuous conduction mode (CCM) the input current of the converter never drops to zero, thus featuring the reduced stress of the input voltage source.

Capacitor Assisted Cascaded qZSI

The investigated topologies are presented in Fig. 1. The basic topology of a capacitor assisted cascaded qZSI (CAC qZSI, Fig. 1*a*) could be derived by the adding of one diode (D_2), one inductor (L_3) and two capacitors (C_3 and C_4) to the traditional qZSI with continuous input current [6-8].

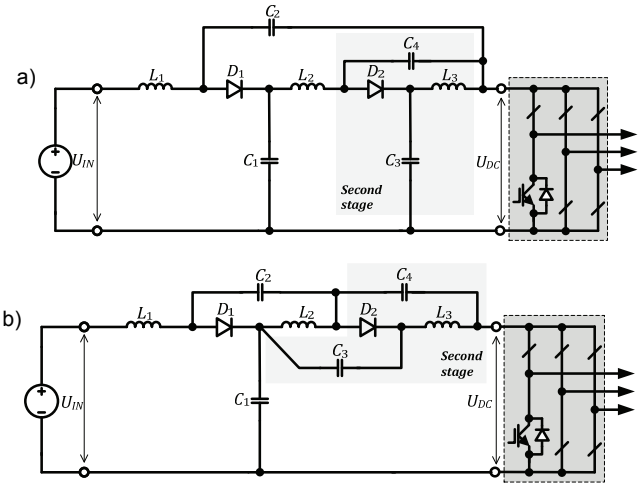


Fig. 1. Capacitor assisted cascaded qZSI topologies: basic CAC qZSI (a) and MCAC qZSI (b).

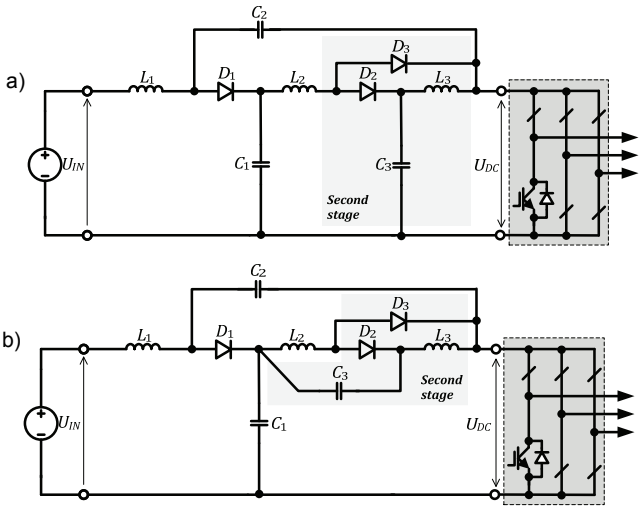


Fig. 2. Diode assisted cascaded qZSI topologies: basic DAC qZSI (a) and MDAC qZSI (b).

The modified topology of a capacitor assisted cascaded qZSI (MCAC qZSI) could be derived from the CAC qZSI simply by the changing of the connection points of capacitors C_2 and C_3, as shown in Fig. 1*b*.

Diode Assisted Cascaded qZSI

The investigated topologies are presented in Fig. 2. The basic topology of a diode assisted cascaded qZSI (DAC qZSI, Fig. 2*a*) could be derived by the adding of one capacitor (C_3), one inductor (L_3) and two diodes (D_2 and D_3) to the traditional qZSI with continuous input current. The modified topology of a diode assisted cascaded qZSI (MDAC qZSI) could be derived from the DAC qZSI simply by the changing of the connection points of the capacitor C_3, as shown in Fig. 2*b*.

Steady State Analysis of Cascaded qZSIs

Generally, the topologies shown in Figs. 1 and 2 could be represented by the PWM inverter coupled with the cascaded qZS-network. In the same manner as the traditional qZSI, the cascaded qZSI has two types of operational states at the dc side: the non-shoot-through states (i.e., the six active states and two conventional zero states of the traditional three-phase voltage source inverter) and the shoot-through state (i.e., both switches in at least one phase conduct simultaneously) [7]. To simplify the analysis the inverter bridge was replaced by a switch *S* (Fig. 3). When the switch *S* is closed, the shoot-through state occurs and the converter performs the voltage boost action. When the switch *S* is open, the active (non-shoot-through) state emerges and previously stored magnetic energy in turn provides the boost of voltage seen on the load terminals.

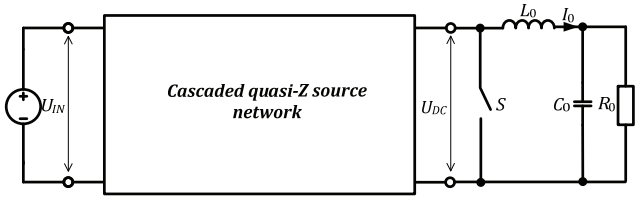


Fig. 3. Simplified power circuit of the cascaded qZSI used in the analysis.

The operating period of the qZS-converter in the CCM generally consists of a shoot-through state t_S and an active (non-shoot-through) state t_A:

$$T = t_A + t_S . \tag{1}$$

Equation (1) could also be represented as

$$\frac{t_A}{T} + \frac{t_S}{T} = D_A + D_S = 1 , \tag{2}$$

where D_A and D_S are the duty cycles of an active and shoot-through states, correspondingly.

Capacitor Assisted Cascaded qZSI

Fig. 4 shows the equivalent circuits of the CAC qZSI operating in the CCM for the shoot-through (a) and active (b) states. At the steady state the average voltage of the inductors over one operating period is zero:

$$U_{L1} = \int_t^{t+T} u_{L1} dt = 0 ; \quad U_{L2} = \int_t^{t+T} u_{L2} dt = 0 ; \quad U_{L3} = \int_t^{t+T} u_{L3} dt = 0 . \tag{3}$$

Based on that fact and defining the shoot-through duty cycle as D_S and the non-shoot-through duty cycle as *(1-*D_S*)*, the inductors' voltages over one operating period could be represented as

$$\begin{cases} U_{L1} = \overline{u}_{L1} = D_S\left(U_{IN} + U_{C2}\right) + \left(1 - D_S\right)\left(U_{IN} - U_{C1}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C4} + U_{C1}\right) + \left(1 - D_S\right)\left(U_{C4} - U_{C2}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C4} + U_{C1}\right) + \left(1 - D_S\right)\left(U_{C1} - U_{C3}\right) = 0 \\ U_{L3} = \overline{u}_{L3} = D_S\left(U_{C3}\right) - \left(1 - D_S\right)\left(U_{C4}\right) = 0 \end{cases} . \tag{4}$$

The peak DC-link voltage is

$$\hat{u}_{DC} = U_{IN} \frac{1}{1 - 3D_S} . \tag{5}$$

The boost ratio of the input voltage is

$$B = \frac{\hat{u}_{DC}}{U_{IN}} = \frac{1}{1 - 3D_S} . \tag{6}$$

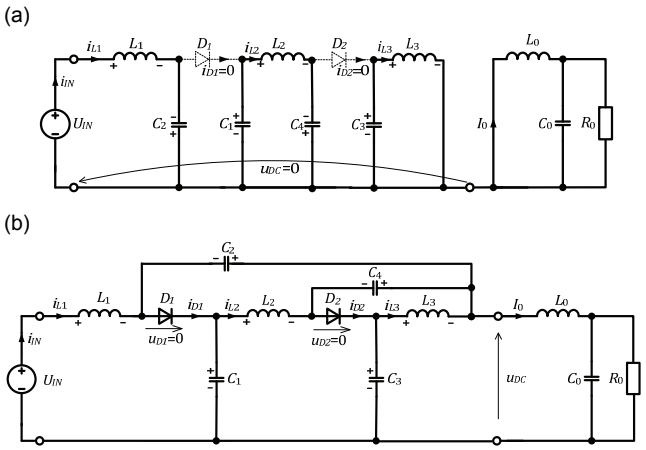


Fig. 4. Equivalent circuits of the CAC qZSI: during the shoot-through state (a) and during the active state (b).

Fig. 5 shows the equivalent circuits of the MCAC qZSI operating in the CCM for the shoot-through (a) and active (b) states.

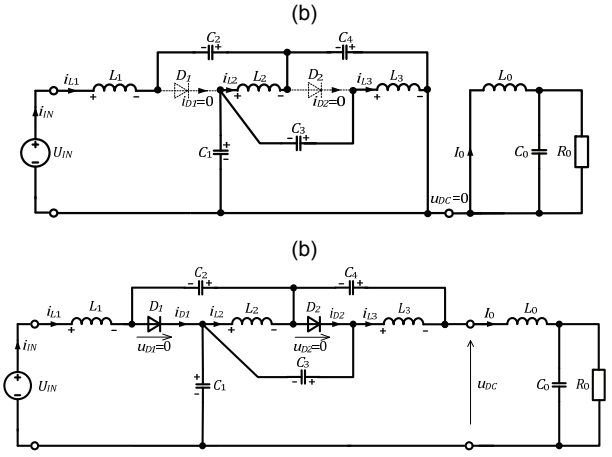


Fig. 5. Equivalent circuits of the MCAC qZSI: during the shoot-through state (a) and during the active state (b).

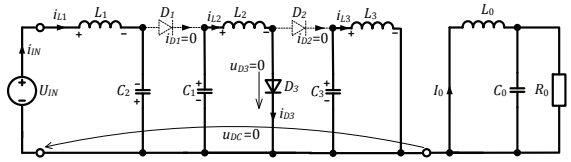
Based on (3) and defining the shoot-through duty cycle as D_S and the non-shoot-through duty cycle as *(1-*D_S*)*, the inductors' voltages over one operating period could be represented as

$$(7)\quad \begin{cases} U_{L1} = \overline{u}_{L1} = D_S\left(U_{IN} + U_{C2} + U_{C4}\right) + \left(1 - D_S\right)\left(U_{IN} - U_{C1}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C4} + U_{C1}\right) + \left(1 - D_S\right)\left(-U_{C2}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C4} + U_{C1}\right) + \left(1 - D_S\right)\left(-U_{C3}\right) = 0 \\ U_{L3} = \overline{u}_{L3} = D_S\left(U_{C3} + U_{C1}\right) + \left(1 - D_S\right)\left(-U_{C4}\right) = 0 \end{cases}.$$

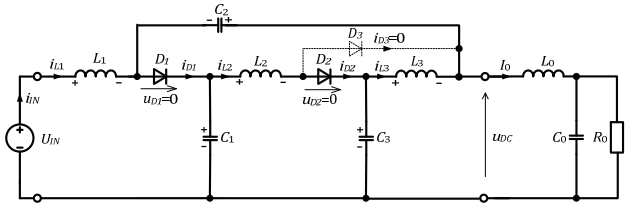
The peak DC-link voltage is and the boost ratio of the input voltage of the MCAC qZSI is exactly the same as of the CAC topology (Eqs. (5) and (6), correspondingly).

Diode Assisted Cascaded qZSI

Fig. 6 shows the equivalent circuits of the DAC qZSI operating in the CCM for the shoot-through (a) and active (b) states.



(a)



(b)

Fig. 6. Equivalent circuits of the DAC qZSI: during shoot-through state (a) and during the active state (b).

Based on (3) and defining the shoot-through duty cycle as D_S and the non-shoot-through duty cycle as $(1\text{-}D_S)$, the inductors' voltages over one operating period could be represented as

$$(8)\quad \begin{cases} U_{L1} = \overline{u}_{L1} = D_S\left(U_{IN} + U_{C2}\right) + \left(1 - D_S\right)\left(U_{IN} - U_{C1}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C1}\right) + \left(1 - D_S\right)\left(U_{C1} - U_{C3}\right) = 0 \\ U_{L3} = \overline{u}_{L3} = D_S\left(U_{C3}\right) + \left(1 - D_S\right)\left(U_{C3} - U_{C1} - U_{C2}\right) = 0 \end{cases}.$$

The peak DC-link voltage is

$$(9)\quad \hat{u}_{DC} = U_{IN}\frac{1}{D_S^2 - 3D_S + 1}.$$

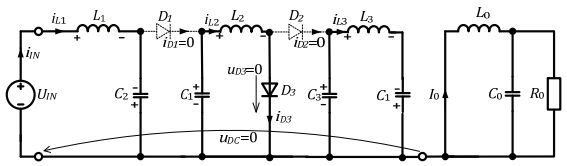
The boost ratio of the input voltage is

$$(10)\quad B = \frac{\hat{u}_{DC}}{U_{IN}} = \frac{1}{D_S^2 - 3D_S + 1}.$$

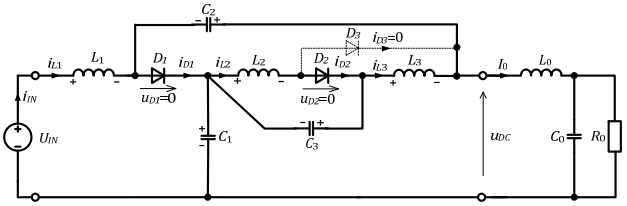
Fig. 7 shows the equivalent circuits of the MDAC qZSI operating in the CCM for the shoot-through (a) and active (b) states. Based on (3) and defining the shoot-through duty cycle as D_S and the non-shoot-through duty cycle as $(1\text{-}D_S)$, the inductors' voltages over one operating period could be represented as

$$(11)\quad \begin{cases} U_{L1} = \overline{u}_{L1} = D_S\left(U_{IN} + U_{C2}\right) + \left(1 - D_S\right)\left(U_{IN} - U_{C1}\right) = 0 \\ U_{L2} = \overline{u}_{L2} = D_S\left(U_{C1}\right) + \left(1 - D_S\right)\left(-U_{C3}\right) = 0 \\ U_{L3} = \overline{u}_{L3} = D_S\left(U_{C3} + U_{C1}\right) + \left(1 - D_S\right)\left(U_{C3} - U_{C2}\right) = 0 \end{cases}.$$

The peak DC-link voltage is and the boost ratio of the input voltage of the MDAC qZSI is exactly the same as of the DAC topology (Eqs. (9) and (10), correspondingly).



(a)



(b)

Fig. 7. Equivalent circuits of the MDAC qZSI: during the shoot-through state (a) and during the active state (b).

Comparison of Operating Properties of Different Cascaded qZSI Topologies

Voltage boost properties

Generally, capacitor assisted and diode assisted cascaded qZSIs have common advantages, such as continuous input current and increased boost factor of the input voltage for the same value of the shoot-through duty cycle as with the traditional qZSI [1-3]. Moreover, in the lossless approach the CAC and MCAC qZSIs could ensure up to 1.25 times higher boost than that of DAC and MDAC topologies (Fig. 8).

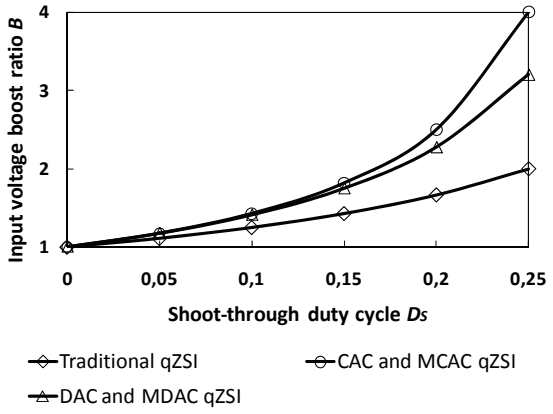


Fig. 8. Comparison of idealized boost properties of capacitor assisted and diode assisted cascaded qZSIs

Operating voltages of capacitors in qZS-networks

The central idea of the modified cascaded qZSIs is to reduce the operating voltages of capacitors in the qZS-network. Thus, by changing the interconnection points of capacitors C_2 and C_3 (as shown in Fig. 1*b*) the CAC qZSI could be easily transformed to the MCAC qZSI, which will feature significantly reduced voltage of capacitor C_3. Moreover, the voltages of capacitors $C_2 \ldots C_4$ will be equalized. In the similar way, simply by changing the connection points of the capacitor C_3 of the DAC qZSI (see Fig. 2*b*) its operating voltage could be decreased by more than six times. The average values of capacitor voltages in different cascaded qZSIs are compared in Table 1.

Table 1. Average voltages of capacitors in different cascaded qZSIs

Capacitors	*Average voltage, V*			
	CAC qZSI	***MCAC qZSI***	***DAC qZSI***	***MDAC qZSI***
C_1	$U_{IN}\frac{1-2D_S}{1-3D_S}$	$U_{IN}\frac{1-2D_S}{1-3D_S}$	$U_{IN}\frac{D_S^2-2D_S+1}{D_S^2-3D_S+1}$	$U_{IN}\frac{D_S^2-2D_S+1}{D_S^2-3D_S+1}$
C_2	$U_{IN}\frac{2D_S}{1-3D_S}$	$U_{IN}\frac{D_S}{1-3D_S}$	$U_{IN}\frac{2D_S-D_S^2}{D_S^2-3D_S+1}$	$U_{IN}\frac{2D_S-D_S^2}{D_S^2-3D_S+1}$
C_3	$U_{IN}\frac{1-D_S}{1-3D_S}$		$U_{IN}\frac{1-D_S}{D_S^2-3D_S+1}$	$U_{IN}\frac{D_S-D_S^2}{D_S^2-3D_S+1}$
C_4	$U_{IN}\frac{D_S}{1-3D_S}$		--------	--------

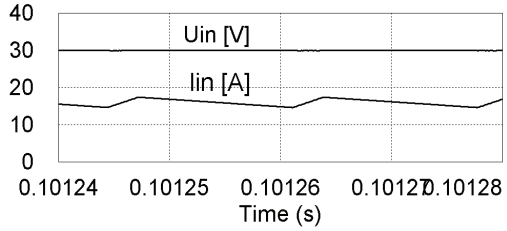
Analysis of Simulation Results

To verify theoretical assumptions a number of simulations were performed by the help of PSIM simulation software. The proposed cascaded qZSI topologies were evaluated with the switching frequency f=30 kHz and shoot-through duty cycle D_S=0.167. The input voltage was set at 30 V and the load resistor selected was 5 Ω. To simplify the analysis losses in the components were neglected. Capacitors and inductors selected for the qZS-networks have the following parameters:

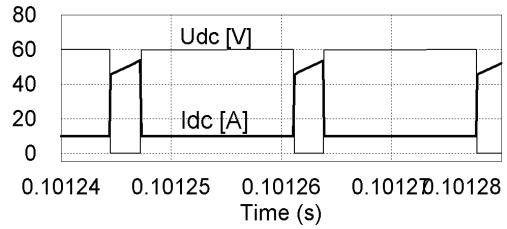
$L_1 \ldots L_3$ = 65 uH;
$C_1 \ldots C_4$ = 180 uF.

Capacitor Assisted Cascaded qZSIs

Fig. 9 shows the general operating waveforms of the CAC and MCAC qZSI topologies. As expected, both converters operate normally, producing twofold boost of the input voltage (U_{IN}=30 V, U_{DC}=60 V, Figs. 9*a* and 9*b*). Moreover, both topologies ensure the continuous input current (Fig. 9*a*) in the CCM.



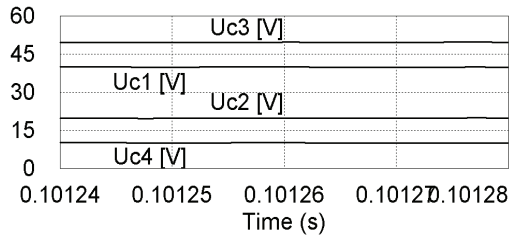
(a)



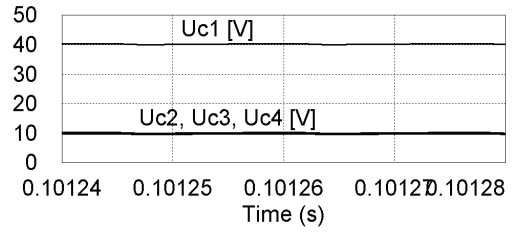
(b)

Fig. 9. Simulated waveforms of the CAC and MCAC qZSIs: input voltage and current (a) and DC-link voltage and current (b).

Fig. 10 shows the operating voltage profiles of capacitors in CAC and MCAC qZSIs. The average values of capacitor voltages are compared in Table 2. It shows that by changing the interconnection points of capacitors C_2 and C_3, as in Fig. 1*b*, the operating voltage of the capacitor C_3 was reduced by five times. Moreover, the voltages of capacitors $C_2 \ldots C_4$ are equalized now.



(a)



(b)

Fig. 10. Capacitor voltages: CAC qZSI (a) and MCAC qZSI (b).

Table 2. Comparison of average voltages of capacitors in CAC and MCAC qZSIs

Capacitors	Average operating voltages	
	CAC qZSI	MCAC qZSI
C_1	39.9 V	40.4 V
C_2	19.8 V	9.8 V
C_3	49.6 V	9.8 V
C_4	10.1 V	10.3 V

Diode Assisted Cascaded qZSIs

Fig. 11 shows the general operating waveforms of the DAC and MDAC qZSIs. Both converters operate normally, producing the demanded boost of the input voltage (U_{IN}=30 V; U_{DC}=57 V, Figs. 11*a* and 11*b*). As expected, both topologies ensure the continuous input current (Fig. 11*a*) in the CCM.

Fig. 12 shows the operating voltage profiles of capacitors in DAC and MDAC qZSI topologies. The average values of capacitor voltages are compared in Table 3. It shows that by changing the interconnection points of the capacitor C_3 (Fig. 2*b*), its operating voltage could be decreased by more than six times.

Table 3. Comparison of average voltages of capacitors in DAC and MDAC qZSIs

Capacitors	Average operating voltages	
	DAEB qZSI	MDAEB qZSI
C_1	39.5 V	39.5 V
C_2	17.2 V	17.4 V
C_3	47.4 V	7.7 V

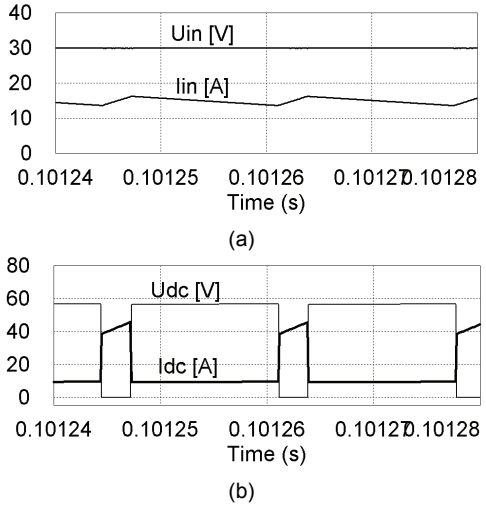


Fig. 11. Simulated waveforms of the DAC and MDAC qZSIs: input voltage and current (a) and DC-link voltage and current (b)

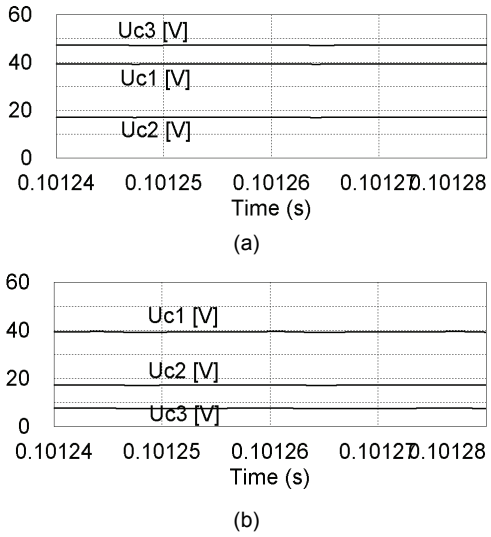


Fig. 12. Capacitor voltages: DAC qZSI (a) and MDAC qZSI (b).

In Fig. 13 the operating waveforms of the diode D_3 (see Fig. 2 for details) are presented. It is shown that for the discussed application the low-voltage low-power fast recovery or the Schottky diode could be used.

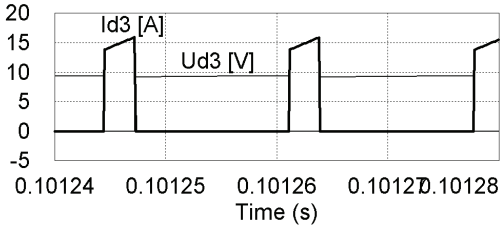


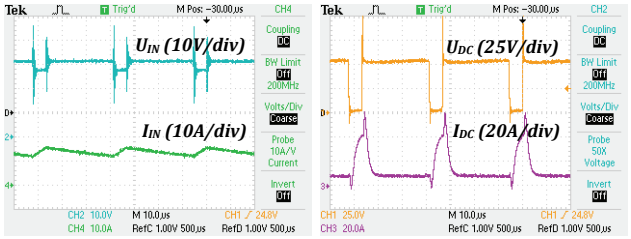
Fig. 13. Operating voltage and current of diode D_3.

Experimental Results

In order to verify theoretical assumptions the laboratory setups corresponding to the investigated topologies were assembled. 600 V/200 A IGBT with extra low saturation voltage was selected for *S* (Fig. 3). Components used in the qZS-networks had the following properties:

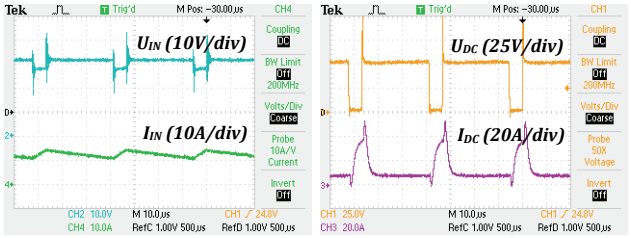
$L_1 \ldots L_3$ = 50 uH; R_L=3 mΩ; type: toroidal inductors;
$C_1 \ldots C_4$ = 180 uF; type: polypropylene capacitors;
$D_1 \ldots D_3$ = 100 V/80 A power Schottky diodes.

In the first experiment, main operating waveforms of the proposed topologies were acquired and compared. The shoot-through duty cycle was set at 0.167. As seen from Fig. 14*b*, due to the losses in the components of the qZS-network both of the capacitor assisted topologies could provide only a 90% of a theoretically predicted input voltage gain (DC-link voltage amplitude 54 V instead of 60V). In the case of diode assisted topologies (Fig 15*b*) the practical voltage gain for the same operating conditions was reduced by 9% in comparison with the theoretically predicted (DC-link voltage amplitude 52 V instead of 57 V).



(a) (b)

Fig. 14. Experimental waveforms of input voltage and current (a) and DC-link voltage and current (b) of the CAC and MCAC qZSIs.



(a) (b)

Fig. 15. Experimental waveforms of input voltage and current (a) and DC-link voltage and current (b) of the DAC and MDAC qZSIs.

During the second experiment the boost properties of the proposed topologies were experimentally verified and compared with theoretical results. In the conditions of fixed input voltage (30 V) and constant load (5 Ω), the shoot-through duty cycle of the converters was increased step by step from 0 to 0.25.

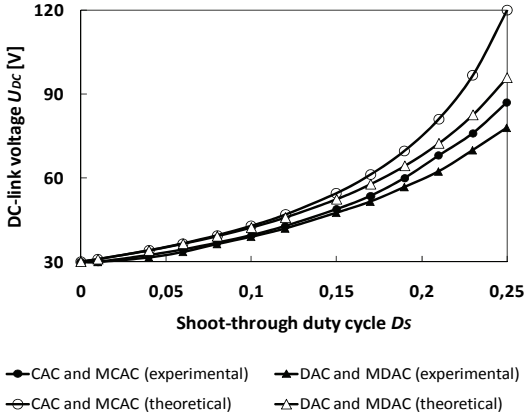


Fig. 16. Theoretical and practical boost properties of the proposed topologies.

Fig. 16 shows that all of the presented topologies suffer from the boost factor reduction, which is mostly caused by the losses in the inductors and diodes of the qZS-network as well as by voltage drops in the interconnection wires. In order to achieve higher possible voltage gain and efficiency these problematic issues should be first addressed during the design routine of cascaded qZSIs. Another interesting

fact is that all four topologies have demonstrated identical boost properties within the shoot-through duty cycle range of 0…0.15, which could be considered during proper topology selection for different applications.

Due to the presence of the input inductor L_1 all the proposed topologies feature the continuous input current in the CCM, as predicted in the analysis. It means that in the CCM the input current never drops to zero during the shoot-through states, thus featuring the reduced stress of the input voltage source, which is especially topical in such demanding applications as power conditioners for fuel cells and solar panels. However, in the case of small loads, relatively low switching frequency and low inductance values of $L_1…L_3$ the proposed converters could start to operate in the discontinuous conduction mode (DCM) and the input current falls to zero during some part of the switching period. This DCM operating mode causes the *overboost effect* of the DC-link voltage, which can lead to instabilities of the converter and must also be taken into account during the sizing of converter components.

To demonstrate the overboost effect of the DC-link voltage the proposed topologies were tested in light load operating conditions when the DCM occurs. The converter was loaded by a 33 Ω resistor and the shoot-through duty cycle was increased step by step from 0 to 0.25. The results of the experiment are presented in Fig. 17. It was stated that the overboost effect is most pronounced in the DAC and MDAC qZSIs with the shoot-though duty cycle D_S lying in the range from 0.04 to 0.24 (Fig. 17*b*). In the case of CAC and MCAC qZSIs the maximal voltage overboost was 11% from that theoretically predicted while in the case of DAC and MDAC qZSIs the maximum overboost reached was 20%. In practice, this undesirable effect can be compensated with appropriately chosen inductances and switching frequencies.

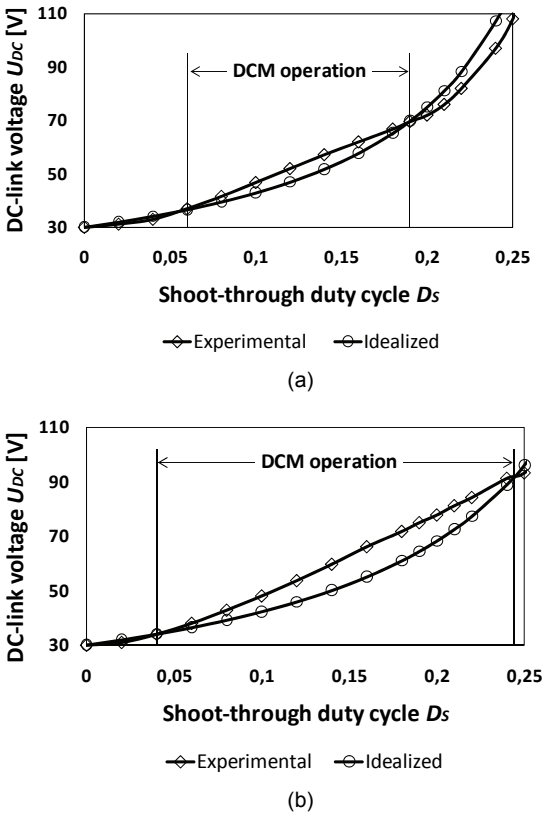


Fig. 17. Transition from CCM to DCM operation: CAC and MCAC qZSIs (a); DAC and MDAC qZSIs (b).

Conclusions

In this paper four cascaded qZSI topologies were proposed, discussed and compared. These topologies were classified as capacitor assisted and diode assisted. A steady state analysis of topologies operating in the continuous conduction mode was performed. Theoretical study was validated by the simulations and experiments. Moreover, some problematic issues of proposed topologies were pointed out and discussed.

It was experimentally stated that in similar operating conditions the discussed topologies provide an identical boost factor of the input voltage within the shoot-through duty cycle range of 0…0.15. Thanks to the presence of the input inductor L_1 all the discussed cascaded qZSIs have continuous input current in the CCM, thus featuring the reduced stress of the input voltage source.

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REFERENCES

[1] Anderson, J.; Peng, F.Z. Four quasi-Z-Source inverters, *IEEE Power Electronics Specialists Conference PESC'2008*, pp. 2743-2749, 15-19 June 2008.

[2] Yuan Li; Anderson, J.; Peng, F.Z.; Dichen Liu Quasi-Z-Source Inverter for Photovoltaic Power Generation Systems, *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition APEC'09*, pp.918-924, 15-19 Feb. 2009.

[3] Jong-Hyoung Park; Heung-Geun Kim; Eui-Cheol Nho; Tae-Won Chun; Jaeho Choi Grid-Connected PV System Using a Quasi-Z-Source Inverter, *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition APEC'09*, pp.925-929, 15-19 Feb. 2009.

[4] W.-Toke Franke, Malte Mohr, Friedrich W. Fuchs Comparison of a Z-Source Inverter and a Voltage-Source Inverter Linked with a DC/DC Boost-Converter for Wind Turbines Concerning Their Efficiency and Installed Semiconductor Power, *IEEE Conf. PESC'08*, pp. 1814 - 1820, June 2008.

[5] C. J. Gajanayake, F. L. Luo, H. B. Gooi, P. L. So, L. K. Siow Extended boost Z-source inverters, *IEEE Conf. ECCE'09*, pp. 3845-3850, Sept. 2009.

[6] M. Adamowicz, R. Strzelecki, D. Vinnikov Cascaded Quasi-Z-Source Inverters for Renewable Energy Generation Systems, *Ecologic Vehicles and Renewable Energies Conference EVER'10*, March 2010.

[7] D. Vinnikov, I. Roasto, R. Strzelecki, M. Adamowicz Performance Improvement Method for the Voltage-Fed qZSI with Continuous Input Current. *IEEE Mediterranean Electrotechn. Conf. MELECON'10*, April 2010.

[8] Vinnikov, D.; Roasto, I.; Jalakas, T. Comparative Study of Capacitor-Assisted Extended Boost qZSIs Operating in CCM. *12th Biennial Baltic Electronic Conf. BEC'2010*, Oct. 2010.

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