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Simple Three-level Neutral Point Voltage Balance Control Scheme Based on Carrier Overlapping SPWM

Abstract. *To address the neutral point voltage balance problem of the diode clamped three-level inverter, this paper analyzes the causes of unbalanced neutral point voltage and studies the impact of the carriers' overlap on the neutral point voltage. A simple neutral point voltage control scheme using carrier overlapping sinusoidal pulse width modulation (SPWM) is proposed. The proposed scheme does not change the modulation waves, the amplitude of one carrier is increased to overlap the other carrier, and the neutral point voltage can be maintained balance by increasing the carriers' amplitudes. The influence of the vertical overlap of carriers on neutral point balance is investigated in depth. The relationship among the neutral point voltage variation, modulation index, overlap of the carriers, and power factor is discussed in this paper. Simulation results show the neutral point voltage balancing control strategy based on SPWM is effective.*

Streszczenie. *W artykule omówiono możliwe przyczyny niezbalansowania napięcia punktu neutralnego w przekształtniku z diodami poziomującymi oraz wpływ na to napięcie nakładania się fal nośnych w modulacji. W przedstawionym schemacie modulacji nakładanie się fal jest wynikiem zwiększenia amplitudy jednej z tych fal. Przedstawiono dyskusję wpływu proponowanej techniki na zmiany napięcia punktu neutralnego oraz zależności między współczynnikiem modulacji, stopniem nakładania się fal i współczynnikiem mocy. Wyniki badań symulacyjnych potwierdzają skuteczność działania. (**Prosta struktura modulacji SPWM z nakładającymi się falami nośnymi do balansowania napięciem punktu neutralnego w przekształtniku trójpoziomowym**)*

Keywords: three-level inverter; neutral point voltage balancing control; carrier overlapping; SPWM
Słowa kluczowe: falownik trójpoziomowy, balansowanie napięciem punktu neutralnego, fala nośna, nakładanie się, SPWM.

Introduction

Recently, there is a growing demand for high-power conversion systems with high output voltage and low harmonics. Since the multilevel inverters have many advantages, including higher voltage capability with the same switching devices, higher quality output voltages and currents, they have been receiving much attention in high-power applications, such as industrial drive, traction and power system, lower switching frequency and lower harmonic contents of the output waveform [1]-[4]. Many multilevel inverter topologies have been proposed, and one of the most popular topology is the neutral point clamped (NPC) three-level inverter. Fig. 1 shows the NPC three-level inverter topology.

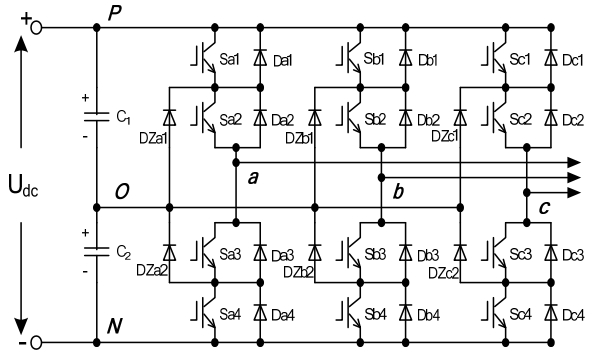


Fig.1. Three-level NPC inverter structure diagram

However, in NPC three-level inverter, the DC-link voltage is divided by capacitors, the current flowing out or into the neutral point can result in the unbalance of the neutral point. Unbalance of the neutral point potential is an inherent problem in NPC three-level inverters. The specific reasons of neutral point voltage unbalance can be attributed to non-uniform DC-link capacitors, operating conditions, and load types. Neutral point voltage unbalance increases output voltage harmonics, may drift the output voltage to unacceptable level, and may damage the switching devices and filter capacitors [5]-[9]. Therefore, various control strategies to maintain the neutral point voltage balance have been proposed in literature. In SPWM scheme, a zero sequence signal is added to the modulation waves to balance the neutral point voltage [10]-[13]. In [10], two auxiliary waves generated by the command voltage were used to produce the control signals. To increase the modulation region, a third harmonic voltage was added to the commanded voltages. The bias term were added to the commanded voltages to balance the neutral point voltage even at high modulation index. In [11], a real-time neutral point voltage control scheme based on zero sequence voltage injection without measuring the power factor angle was proposed. The neutral point voltage can be controlled precisely thereby completing suppressing the ripple. However, a large number of parameters are used in the calculations of the schemes, making them unsuitable for instantaneous control.

In the paper, a neutral point voltage balance control scheme based on carrier overlapping SPWM is proposed. A comprehensive analysis of the neutral point voltage variation based on neutral point current is presented in the paper. For the new strategy, amplitudes of the carriers are increased, the neutral point voltage variation is correlative with the modulation index, overlap of the carriers, power factor angle, and load current value. The neutral point voltage can be balanced by adjusting the overlap of the carriers with different power factors. Simulation results show that the strategies have good capability for neutral point voltage balance.

Neutral point balancing analysis of SPWM scheme

Many modulation schemes exist for generating PWM signals. The SPWM modulation scheme is the most widely used method because it can be easily implemented using digital techniques and extended for higher-level converter topologies. The multilevel SPWM modulation scheme is based on a comparison of a sinusoidal reference waveform with several vertically shifted carrier waveforms. The SPWM scheme for there-level inverter is shown in Fig. 2, during a PWM period, if the modulation wave is greater than the upper carrier wave, switch Sa1 is on and Sa3 is off. In contrast, if the modulation wave is greater than the lower carrier wave, switch Sa2 is on and Sa4 is off. There are three output states of phase voltage. When Sa1 and Sa2 are on, Sa3 and Sa4 are off, the output state is "P", the phase voltage U_{aO} = U_{dc}/2. Output state "O" signifies that

Sa2 and Sa3 are on, Sa1 and Sa4 are off, U_{aO} = 0. When Sa3 and Sa4 are on, Sa1, Sa2 are off, the output state is "N" and U_{aO} =-U_{dc}/2.

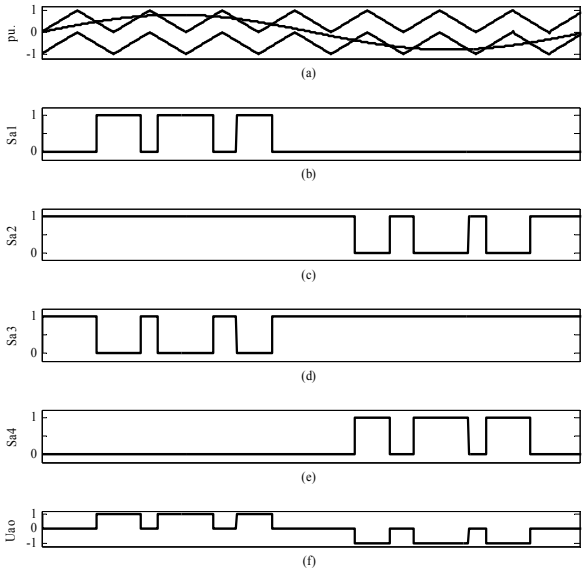


Fig.2. (a) SPWM scheme for three-level NPC inverter, (b)-(e) the gate signals for switches Sa1, Sa2, Sa3, and Sa4, (f) output phase voltage

The three phase reference voltages are expressed by following expressions, where m is the modulation index, 0≤m≤1.

$$(1)\qquad \begin{cases} u_a = m\sin\omega t \\ u_b = m\sin(\omega t - \frac{2}{3}\pi) \\ u_c = m\sin(\omega t - \frac{4}{3}\pi) \end{cases}$$

The output currents are assumed as sinusoidal:

$$(2)\qquad \begin{cases} i_a = I_m\sin(\omega t - \varphi) \\ i_b = I_m\sin(\omega t - \frac{2}{3}\pi - \varphi) \\ i_c = I_m\sin(\omega t - \frac{4}{3}\pi - \varphi) \end{cases}$$

where I_m is the current amplitude, φ is the power factor angle, and ω is the fundamental angular frequency.

The carrier frequency is assumed to be sufficiently high compared with the output frequency, whereas the reference voltages and phase currents are assumed constant in a PWM period.

The average neutral point current during a PWM period is

$$(3)\qquad i_o = i_a d_{ao} + i_b d_{bo} + i_c d_{co}$$

where d_{jo} (j=a, b, c) is the time ratio of the "O" state in each PWM period. As shown in Fig. 3, when $u_j \geq 0$, if $u_{tri1} > u_j$, the output state is "O" and t_{jo}=(1-u_j)×T. When $u_j < 0$, if $u_{tri2} < u_j$, the output state is "O" and t_{jo}=(1+u_j)×T, where u_{tri1} is the upper carrier; u_{tri2} is the lower carrier for three-level SPWM algorithm, t_{jo} is the dwelling time of the "O" state, and the PWM period is T, hence, the time ratio of the "O" state is shown by the following expression:

$$(4)\qquad d_{jo} = \begin{cases} 1-u_j & (u_j \geq 0) \\ 1+u_j & (u_j < 0) \end{cases}$$

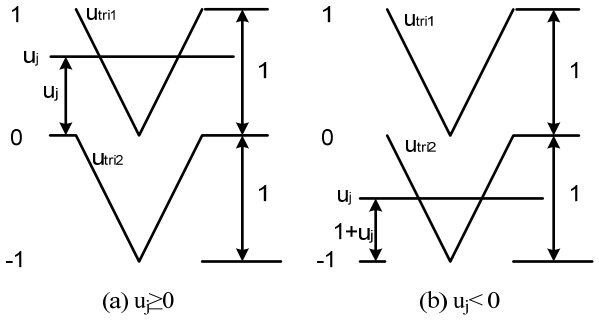


Fig.3. Time ratio of the "O" state

The relationship between the neutral point current i_o and voltage unbalance dU_c is

$$(5)\qquad dU_c = U_{c1} - U_{c2} = \frac{i_o}{C} = \frac{i_a d_{ao} + i_b d_{bo} + i_c d_{co}}{C}$$

When any phase is clamping to the neutral point, the current flows out or into the neutral point, which results in a rippling of the capacitor voltages and the neutral point unbalance.

Neutral point balance control

Various SPWM schemes have been proposed for neutral point unbalance of NPC inverter. However, most of these schemes are based on modulation waves. A carrier overlapping SPWM scheme based on carriers is proposed in this paper for neutral point balance control. Maintaining the neutral voltage balance can be accomplished by moving the overlap up or down. In the scheme, the period of the carriers is not changed, whereas the amplitudes of the carriers are changed. Let h be the vertical overlap of the carriers. The overlap of the carriers, when the amplitude of upper carrier increases to 1+h, is shown in Fig. 4.

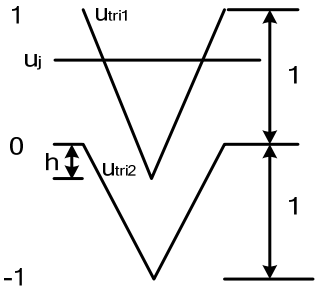


Fig.4. Time ratio of the "O" state when the amplitude of upper carrier increases

When the carrier changes, the "O" state action time becomes

$$(6)\qquad d'_{jo} = \begin{cases} (1-u_j)/(1+h) & (u_j \geq 0) \\ (1+u_j \times h)/(1+h) & (-h < u_j < 0) \\ 1+u_j & (u_j \leq -h) \end{cases}$$

Let dU_{cj} (j=a, b, c) be the change in the neutral point voltage caused by each phase. The expression of dU_{ca} is then

$$dU_{ca}=\int_0^{2\pi}\frac{i_a d_a'}{C}d(\omega t)=\int_0^{\pi}\frac{i_a}{C}\times\frac{1-u_j}{1+h}d(\omega t)+\int_{\pi}^{\pi+\arcsin(h/m)}\frac{i_a}{C}\times\frac{1+u_j\times h}{1+h}d(\omega t)$$

$$+\int_{\pi+\arcsin(h/m)}^{2\pi-\arcsin(h/m)}\frac{i_a\times(1+u_j)}{C}d(\omega t)+\int_{2\pi-\arcsin(h/m)}^{2\pi}\frac{i_a}{C}\times\frac{1+u_j\times h}{1+h}d(\omega t) \quad (7)$$

$$=-\frac{I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2]$$

Proven by the same methods, dU_{cb} and dU_{cc} are shown by the following expression:

$$dU_{cb}=dU_{cc}=-\frac{I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2] \quad (8)$$

The total change of the neutral point voltage is

$$dU_c=-\frac{3\times I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2] \quad (9)$$

The relationship among dU_c, m and h is shown in Fig. 5. The system is in motoring mode when φ is in (-π/2, π/2), and system is in regenerative mode when φ is in (π/2, 3π/2). Therefore, in motoring mode, when the amplitude of upper carrier u_{tri1} increases, dU_c<0 and neutral point voltage will increase. In regenerative mode, when the amplitude of upper carrier u_{tri1} increases, dU_c>0 and neutral point voltage will decrease.

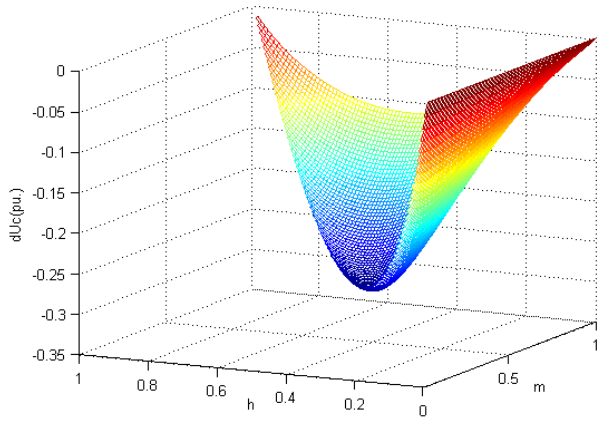


Fig.5. Relationship among dUc, m and h

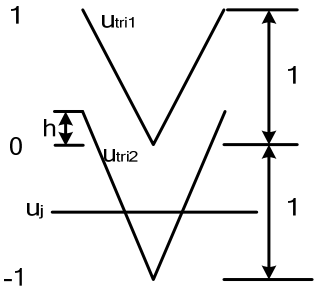


Fig.6. Time ratio of the "O" state when the amplitude of lower carrier increases

The overlap of the carriers, when the amplitude of lower carrier increases to 1+h, is shown in Fig. 6.

When the carriers change, the "O" state action time becomes

$$d'_{jo}=\begin{cases}1-u_j & (u_j\ge h)\\ (1-u_j\times h)/(1+h) & (0<u_j<h)\\ (1+u_j)/(1+h) & (u_j\le 0)\end{cases} \quad (10)$$

The expression of dU_{ca} is

$$dU_{ca}=\int_0^{2\pi}\frac{i_a d_a'}{C}d(\omega t)=\int_0^{\arcsin(h/m)}\frac{i_a}{C}\times\frac{1-u_j\times h}{1+h}d(\omega t)+\int_{\arcsin(h/m)}^{\pi-\arcsin(h/m)}\frac{i_a\times(1-u_j)}{C}d(\omega t)$$

$$+\int_{\pi-\arcsin(h/m)}^{\pi}\frac{i_a}{C}\times\frac{1-u_j\times h}{1+h}d(\omega t)+\int_{\pi}^{2\pi}\frac{i_a}{C}\times\frac{1-u_j}{1+h}d(\omega t) \quad (11)$$

$$=\frac{I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2]$$

When the amplitude of lower carrier increases, proven by the same methods, dU_{cb} and dU_{cc} are shown by the following expression:

$$dU_{cb}=dU_{cc}=\frac{I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2] \quad (12)$$

The total change of the neutral point voltage is

$$dU_c=\frac{3\times I_m\times\cos\varphi}{2\times m\times C\times(1+h)}[2\times h\times\sqrt{m^2-h^2}+2\times m^2\times\arcsin(h/m)-\pi\times h\times m^2] \quad (13)$$

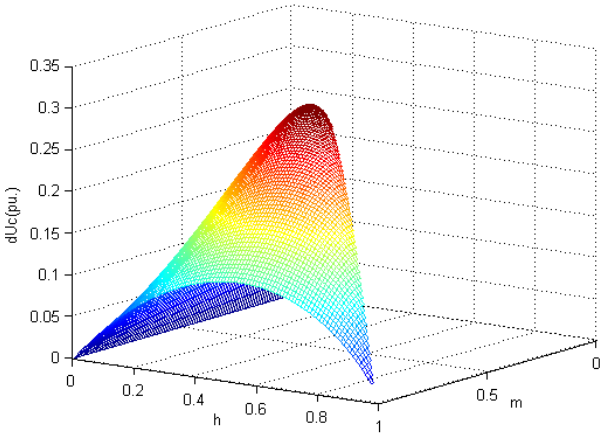
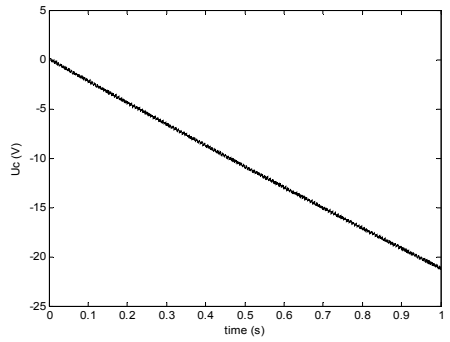


Fig.7. Relationship among dUc, m and h

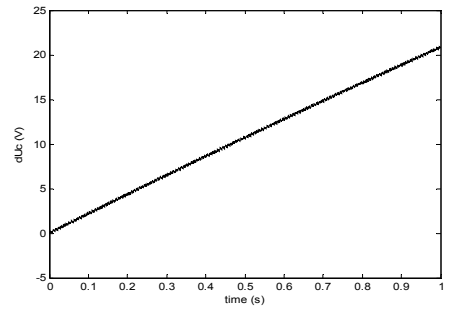
The relationship among dU_c, m and h is shown in Fig. 7. The system is in motoring mode when φ is in (-π/2, π/2), and system is in regenerative mode when φ is in (π/2, 3π/2). Therefore, in motoring mode, when the amplitude of lower carrier u_{tri2} increases, dU_c>0 and neutral point voltage will decrease. In regenerative mode, when the amplitude of lower carrier u_{tri2} increases, dU_c<0 and neutral point voltage will increase. As shown in Fig. 5 and Fig. 7, the absolute change value of the neutral point voltage is proportional to the overlap of carriers, when the power factor angle φ and modulation index m are kept invariant. Hence, maintaining the neutral point balance by increasing the carriers' amplitudes is available, and the adjusting strength can be controlled by the overlap h.

Simulation and result analysis

The validity of the carrier overlapping SPWM scheme is verified through simulations on the three-level NPC inverter using the Matlab Simulink package. In the simulation, the switching frequency is 1kHz and the frequency of sinusoidal reference waveform is 50Hz.

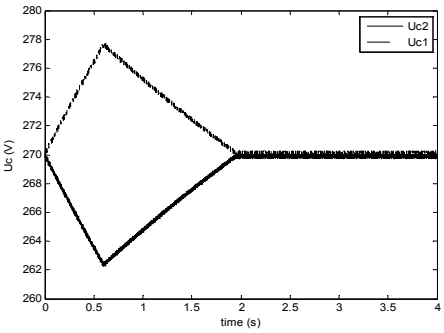


(a) Amplitude of upper carrier increasing

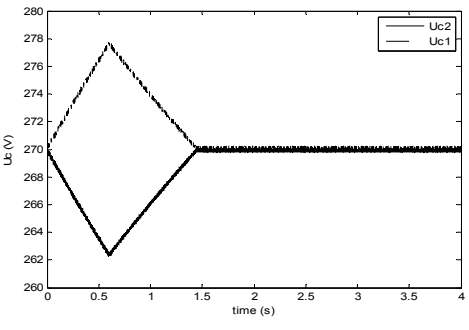


(b) Amplitude of upper carrier increasing

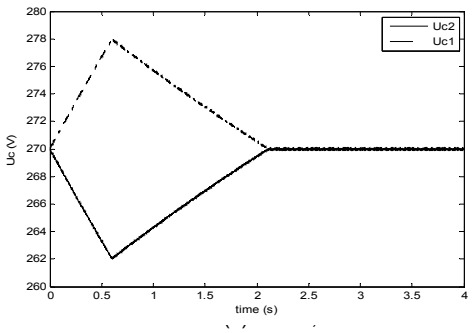
Fig.8. Offset of the neutral point voltage, when m=0.7, h=0.3

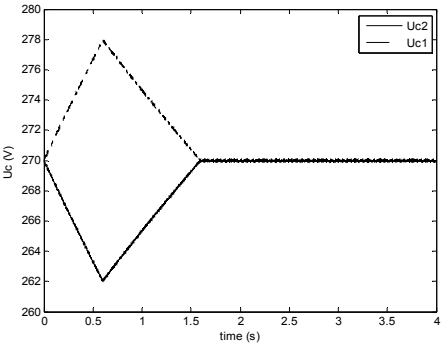


(a) m=0.7, h=0.25



(b) m=0.7, h=0.3

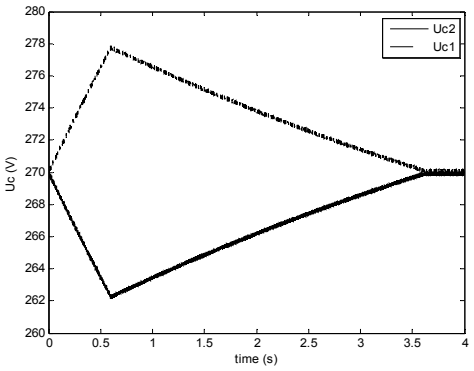




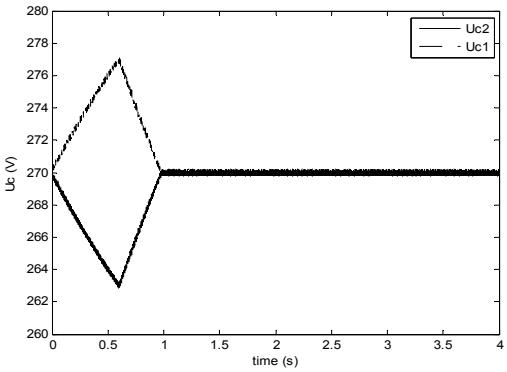
(d) m=0.4, h=0.3

Fig.9. Control results using neutral point control strategy

Fig. 8 shows that the neutral point voltage is initially balanced at dU_c=0; but it drifts over time; h=0.3 is given in the open loop without the feedback of neutral point voltage. When the amplitude of upper carrier increases, the dU_c drops rapidly to -21V in 1s as shown in Fig. 8(a), when the amplitude of lower carrier increases, the dU_c drops rapidly to 21V in 1s as shown in Fig. 8(b). When the amplitude of upper carrier increases, dU_c<0, and when the amplitude of lower carrier increases, dU_c>0, which are consistent with the conclusions of the theoretical analysis.



(a) m=0.7, h=0.3, L=100mH



(b) m=0.7, h=0.3, L=10mH

Fig.10. Control results with different power factors

In the closed-loop control, the DC-link voltage is set to 540V, the initial voltage values of two capacitors are 270V, and the switching frequency is 1kHz. A resistor is placed parallel to C_2 to create the neutral point unbalance, R=1000Ω. The voltage value deviation of two capacitors occurs when the system is working. However, at t=0.6s, the control of the neutral point voltage is applied, the deviation of the two capacitor voltages is suppressed, and neutral

point voltage is quickly balanced. The system is simulated with different modulation indices, overlaps, and power factors. The neutral point voltage control results are shown in Fig. 9 with resistance-inductance load, the resistance is 30Ω, and inductance is 66mH of the load. Fig. 9(a), (b) show the control results when modulation index m is 0.7, the regulation time is 1.35s in Fig. 9(a), and the regulation time is 0.83s in Fig. 9(b). Fig. 9(c), (d) show the control results when modulation index m is 0.4, the regulation time is 1.49s in Fig. 9(c), the regulation time is 0.98s in Fig. 9(d). The results in Fig. 9(a), (c) are obtained when the system is operated with h=0.25, the results in Fig. 9(b), (d) are obtained when the system is operated with h=0.3. It can be noticed that the regulating capacity of the neutral point voltage is markedly strengthened with the increase of the value of h when the modulation index m is kept invariant, which is in complete accordance with the theory.

Fig. 10 shows the relationship between the neutral point voltage regulating capacity of the proposed scheme and power factor, when modulation index is 0.7, and h=0.3. In Fig. 10(a), the resistance is 30Ω, and inductance is 100mH of resistance–inductance load, the neutral point voltage regulation time is 3.04s. In Fig. 10(b), the resistance is 30Ω, and inductance is 10mH of the load, the neutral point voltage regulation time is 0.36s. And as shown in Fig. 9(b), the neutral point voltage regulation time is 0.83s, when the resistance is 30Ω, and inductance is 66mH of the load. The power factor will become higher when the inductance decreases, and the resistance keeps invariant. It can be seen that regulating capacity of the neutral point voltage is markedly strengthened by increasing the power factor with the other parameters consistent, which is consistent with equation (9) and equation (13).

Conclusion

In this paper, a neutral point voltage balance control scheme based on carrier overlapping SPWM for three-level inverters is presented. This scheme maintains the neutral point voltage balance by increasing the carriers' amplitudes. The causes of the neutral point unbalance are studied in detail, and the neutral point voltage variation is correlative with the modulation index, overlap of the carriers, power factor angle, and load current value. The absolute change value of the neutral point voltage is proportional to the overlap of carriers, when the other parameters are kept invariant. The new simple and effective method for neutral point voltage control is verified through simulation. Simulation results show that the proposed strategy presents good performance on neutral point voltage balance control with different power factors.

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