Ning Ning, Zhiling Sui, Hua Chen, Shuangheng Xu, Jun Zhang, Jie Zheng, Shuangyi Wu, Qi Yu

State Key Lab of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China

Transfer characteristic shift technique for full input range in pipelined ADCs with background calibration

Abstract. *A transfer characteristic shift technique has been proposed in this paper. By shifting the transfer characteristic of the sub-stage under calibration in pipelined ADC, a full input range is realized for pipelined ADC with background calibration. Pseudorandom sequence (PN) signal with maximum amplitude of Vref/4 can be injected into the multiplying digital-to-analog converter (MDAC) which speeds up the convergence process. Simulation results shows that the technique can achieve full input range and fast convergence speed simultaneously with small hardware cost in pipelined ADCs with PN signal based background calibration.*

Streszczenie. *W artykule przedstawiono metodę przesunięcia charakterystyki przesyłu potokowych przetworników analogowo-cyfrowych. Badania symulacyjne dowodzą, że proponowana technika pozwala na wykorzystanie pełnego zakresu wejściowego przetwornika oraz szybką konwergencję, przy niewielkich wymaganiach sprzętowych. (**Metoda uzyskania pełnego zakresu wejściowego potokowego przetwornika analogowo-cyfrowego o kalibracji w tle**)*

Keywords: Pipelined ADC background calibration, transfer characteristic shift, full input range, pseudorandom sequence.
Słowa kluczowe: Przetwornik potokowy ADC o kalibracji w tle, przesunięcie charakterystyka przesyłu, pełen zakres wejściowy, sekwencja pseudo-losowa

Introduction

Modern mobile electronic systems are always desired to have high resolution and high speed ADC's with extremely wide dynamic range. In the particular case of Pipelined ADCs, high resolution limited by component mismatch has relied on a variety of circuit calibration techniques to be improved [1].

Generally, calibration techniques can be divided into foreground calibration and background calibration. Foreground calibration technique can be used to achieve high resolution [2, 3, 4], but cannot track variations over time caused by component aging or by temperature and power-supply changes. Background calibration techniques overcome this limitation [5, 6, 7]. However, it needs to occupy the dynamic range of input analog signal [8, 9, 10].

This paper presents a transfer characteristic shift technique. This technique can be applied to pipelined ADC with PN signal based background calibration to achieve full input range. Therefore large amplitude of PN signal can be used for calibration to speed up the convergence process. Only two comparators and one digital adder are needed to accomplish the implementation.

Conventional Background Calibration Technique

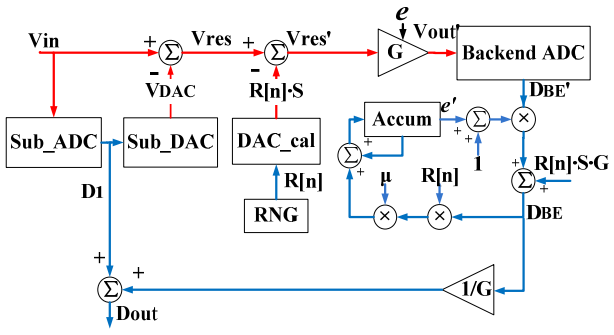

Fig.1. Conventional digital background calibration schematic

Fig.1 shows a conventional digital background calibration schematic. The principle of these techniques is to inject a PN signal, $R[n]\cdot S$, into the stage under calibration[9]. $R[n]$ is zero mean pseudorandom sequence taking on values of ± 1, and S is amplitude. So $R[n]\cdot S$ has a certain amplitude and random polarity with zero mean. This PN signal and input analog signal will be amplified by the stage's residue amplifier together. Assuming that the residue amplifier has an ideal gain of G and a relative gain error e, so the output of this stage V_{out} can be given as

$$V_{out} = G(1+e)(V_{in} - V_{DAC} - R[n]\cdot S) = G(1+e)(V_{in} - V_{DAC}) - G(1+e)(R[n]\cdot S) \quad (1)$$

where: V_{DAC} – the output of sub_DAC.

This output signal consists of two terms, the input analog signal and the PN signal, both carry the gain error. (V_{in}–V_{DAC}) is a variable value, G is a known constant value and (1+e) is an unknown constant value which needs to be measured for calibration. So the key is how to measure the (1+e) from V_{out}.

In equation (1), the first term $G(1+e)(V_{in}-V_{DAC})$ is a variable value which need to be calibrated and output, the second term $G(1+e)R[n]\cdot S$ is a constant value with random polarity which can be measured. V_{out} will be quantified by the backend ADC, and the information carried by V_{out} can be moved into D_{BE}' in digital domain.

$$D_{BE}' = G(1+e)(V_{in} - V_{DAC}) - G(1+e)(R[n]\cdot S) \quad (2)$$

After a series of arithmetic, statistic operation and use of the zero mean feature of $R[n]$, the input analog signal can be almost cancelled and only the constant e will be left to generate the calibration coefficient g_{cal}. This coefficient g_{cal} can be used to calibrate the gain error in analog or digital domain.

Transfer Characteristic Shift Technique

One major problem about the previous background calibration technique is the tradeoff between input signal range and amplitude of PN signal.

In the case of a 1.5bit pipelined ADC stage, its transfer characteristic is shown in Fig.2 with solid line. The residue amplifier output V_{out} can be given as

$$V_{out} = G(V_{in} - V_{DAC}) \quad (3)$$

Taking the PN signal $R[n]\cdot S$ into account, V_{out} becomes V_{out}' as the two dash lines.

$$V_{out}' = G(V_{in} - V_{DAC} - R[n]\cdot S) = G(V_{in} - V_{DAC}) \pm G\left|R[n]\cdot S\right| \quad (4)$$

where: $G|R[n]\cdot S|$ – the PN signal be amplified by the residue amplifier.

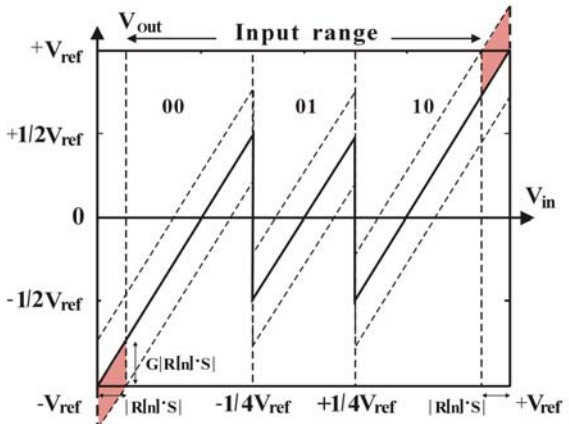

Fig.2. Transfer characteristic of conventional 1.5bit sub_stage ADC

A. Transfer characteristic shift for full input range

To avoid overrange of the residue amplifier, V_{out}' need to be within the range of $\pm V_{ref}$. From equation (4), V_{in} can be obtained as

$$V_{-DAC}+\left|R[n]\cdot S\right|-\frac{V_{ref}}{G}\le V_{in}\le V_{+DAC}-\left|R[n]\cdot S\right|+\frac{V_{ref}}{G} \tag{5}$$

where: V_{-DAC} – the sub_DAC output when V_{in} is below $-V_{ref}/4$, V_{+DAC} – the sub_DAC output when V_{in} is above $+V_{ref}/4$.

In the case of 1.5bit stage showed in Fig.2, G=2, V_{-DAC}=-$V_{ref}/2$, V_{+DAC}=+$V_{ref}/2$, the shaded area is where output over range could occur, so $2|R[n]\cdot S|$ of the input range has been occupied by the calibration signal.

$$-V_{ref}+\left|R[n]\cdot S\right|\le V_{in}\le V_{ref}-\left|R[n]\cdot S\right| \tag{6}$$

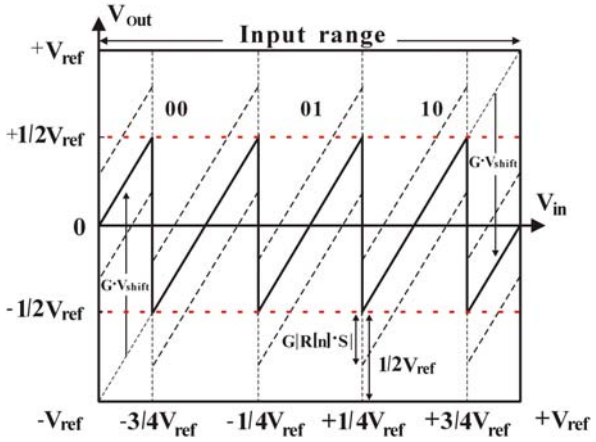

Fig.3. Transfer characteristic of modified 1.5bit sub_stage ADC

Obviously, in a conventional transfer characteristic showed in Fig.2, output overrange is inevitable as long as the calibration use full input range and PN signal simultaneously. To solve this problem, the transfer characteristic can be adjusted as Fig.3 depicted. By shifting the output characteristic away from the boundary with $G\cdot V_{shift}$ which equals to V_{ref}, the output will be within the range of $\pm V_{ref}/2$, so a $V_{ref}/2$ output margin can be created for the amplified PN signal $G|R[n]\cdot S|$ while the full input range is intact. To avoid output over range, $|R[n]\cdot S|$ only need to be less than $V_{ref}/2G$. In a 1.5 bit stage, G=2, $|R[n]\cdot S|<V_{ref}/4$. The shift made in transfer characteristic can be compensated in digital domain and the original signal will be recovered.

B. Fast convergence speed with large PN signal

As equation (2) mentioned, the backend ADC output D_{BE}' consists two terms, the input signal $G(1+e)(V_{in}-V_{DAC})$ and the PN signal $G(1+e)R[n]\cdot S$. These two terms will be used to generate the correct output D_{BE} and calibration coefficient g_{cal} respectively after being processed by the background calibration circuit, as Fig.1 shown. g_{cal} equals to 1 plus the accumulator output e', and e' can be given as

$$\begin{aligned} e' &= \sum \mu\cdot G(1+e)\cdot g_{cal}\cdot\left(V_{in}-V_{DAC}\right)\cdot R[n] \\ &+\sum \mu\cdot G\cdot S\left(1-(1+e)\cdot g_{cal}\right) \end{aligned} \tag{7}$$

where the first term has a zero mean characteristic and it will be cancelled statistically. Only the second term will be accumulated to generate output e'. e' has a magnitude of 10^{-2} which depends on the gain error e. μ should be small enough to suppress the input signal so that a stable calibration coefficient g_{cal} can be generated[5]. The problem is that with a very small μ, the second term we used to accumulate the e' is suppressed as well which will slow down the convergence process.

In the second term $\mu\cdot G\cdot S(1-(1+e)\cdot g_{cal})$, μ has to be small enough to provide a stable g_{cal}, G is determinate by the stage under calibration, and $(1-(1+e)\cdot g_{cal})$ is variable which depends on how close the calibration coefficient approximate to the real gain value. So the amplitude of the PN signal S becomes critical to the convergence speed. The larger the factor S is, the faster the convergence process is. With transfer characteristic shift technique being applied, a PN signal with $S=V_{ref}/4$(In a 1.5bit stage) can be used for calibration, and this will boost the convergence speed significantly.

Circuit Implementation

The residue amplifier output has been given by (8), two comparators with comparative levels $\pm 3V_{ref}/4$ are added, and divide the full input range into 5 areas.

$$V_{out}=\begin{cases} 2\left(V_{in}+\dfrac{V_{ref}}{2}+V_{shift}\right) & \left(V_{in}\le -\dfrac{3V_{ref}}{4}\right) \\ 2\left(V_{in}+\dfrac{V_{ref}}{2}\right) & \left(-\dfrac{3V_{ref}}{4}\le V_{in}<-\dfrac{V_{ref}}{4}\right) \\ 2V_{in} & \left(-\dfrac{V_{ref}}{4}\le V_{in}<\dfrac{V_{ref}}{4}\right) \\ 2\left(V_{in}-\dfrac{V_{ref}}{2}\right) & \left(\dfrac{V_{ref}}{4}\le V_{in}<3V_{ref}/4\right) \\ 2\left(V_{in}-\dfrac{V_{ref}}{2}+V_{shift}\right) & \left(V_{in}\ge\dfrac{3V_{ref}}{4}\right) \end{cases} \tag{8}$$

These two extra comparator's output will be input to the modified sub_DAC as shown in Fig.4. When the input signal is below $-3V_{ref}/4$, a shift signal V_{shift} equals to $V_{ref}/2$ controlled by the lower bits is added to the input signal. When the input signal is above $3V_{ref}/4$, another $-V_{ref}/2$ controlled by the higher bit is added to the input signal. To compensate the shift signal V_{shift} added into the input signal, a digital constant value D_{comp} can be subtracted from the digital output after the conversion process of backend ADC finished. D_{comp} is given as

$$D_{comp}=\frac{V_{shift}}{V_{fullscale}}D_{fullscale} \tag{9}$$

where: $V_{fullscale}$ – the full range of the input analog signal of the given stage, $D_{fullscale}$ – the numeric code correspond to $V_{fullscale}$.

In the case of 1.5bit stage, assuming that it's the first stage of a 12-bits pipelined ADC, and $V_{fullscale}$ =2V_{ref}, |V_{shift}|=V_{ref}/2, and $D_{fullscale}$=2^{12}, D_{comp} = 2^{10}.

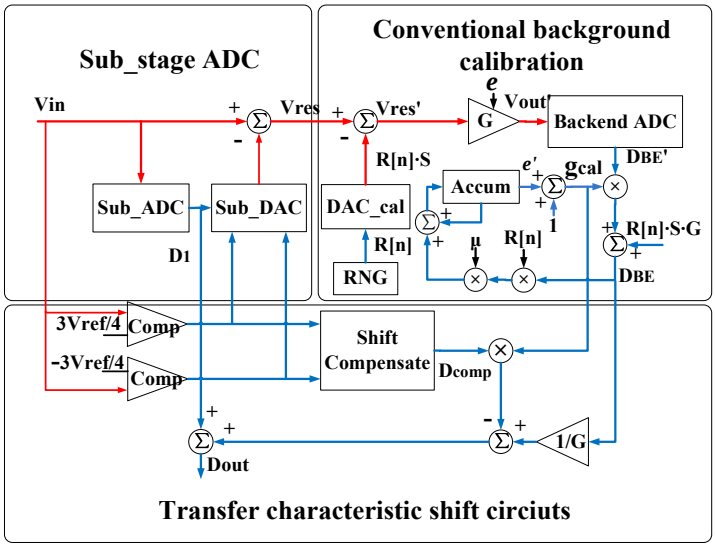

Fig.4. Background calibration with transfer characteristic shift technique

The calibration scheme shown in Fig.4 only adjusts the digital output. The interstage gain error in MDAC is not calibrated, and the V_{shift} amplified by the residue amplifier also contain the gain error, so the D_{comp} need to be calibrated with g_{cal} before we subtract it from the D_{out}. Furthermore, these two comparators added in $\pm 3V_{ref}/4$ could have offset error, and it will be calibrated by the redundancy calibration scheme as well just like any offset error in the two comparators assigned to $\pm V_{ref}/4$. So no side effect will be brought into the system with this technique being applied. But offset error can cause the output over the range of $\pm V_{ref}/2$, and the $V_{ref}/2$ output margin will be occupied partially. So the amplitude of PN signal used should be slightly less than the maximum value.

Simulation Results

The simulation is operated on a 12 bits pipelined ADC with transfer characteristic shift technique. The pipelined ADC consists of nine 1.5 bit stages and one 3 bit flash ADC. The first 1.5 bit stage is the calibrated stage, the following stages work as the backend ADC. The full input range $V_{fullscale}$ is $\pm V_{ref}$ and the correspond digital full output range $D_{fullscale}$=2^{12}, the shift signal |V_{shift}|=V_{ref}/4 and D_{comp} = 2^9.

Fig.5 depicts the digital output waveform of the 12 bit pipelined ADC with a full range input signal. A PN signal with amplitude of V_{ref}/8 is used for calibration. D_{comp} is the compensation signal, D_{out}' is the ADC output without D_{comp}, D_{out} is the ADC output with D_{comp}. Offset in the peak and valley of D_{comp} is caused by V_{shift} added in the modified sub_DAC. The compensation signal D_{comp} is delayed 9 clocks to synchronize with the backend ADCs output. Add D_{comp} to D_{out}' will recover the origin signal D_{out}. As shown in Fig.5, full input range and lager amplitude of calibration signal can be used simultaneously.

Fig.6 depicts the convergence process of calibration coefficient in the 12 bit pipelined ADC with 2% gain error in the first 1.5bit stage. Three PN signal of V_{ref}/8, V_{ref}/16 and V_{ref}/32 are used, and the time cost to convergence are 1040, 1730, 2820 conversion cycles respectively. As shown in Fig.6, the calibration coefficient can approximate the real gain value (1+2%) very accurate, and the larger the amplitude of the PN signal is, the faster the convergence process is.

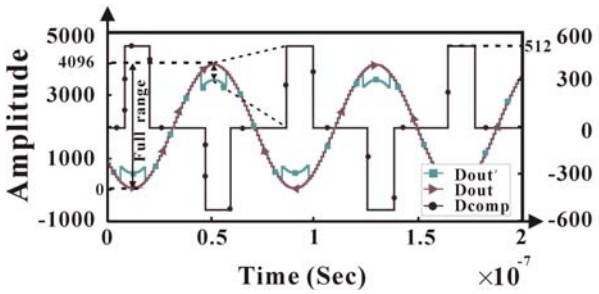

Fig.5. Output waveform of pipelined ADC with transfer characteristic shift

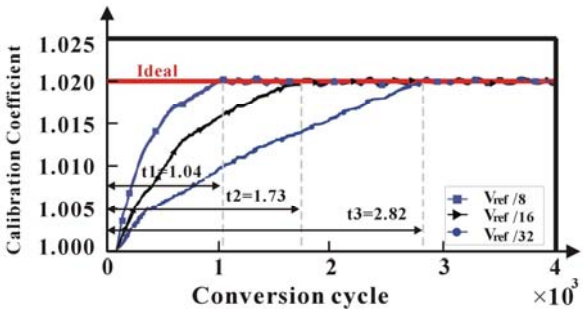

Fig.6. Convergence process of a 1.5 bits stage with PN signal of different amplitude

Conclusion

A transfer characteristic shift technique is proposed. By shifting the transfer characteristic of the stage under calibration, full input signal range is realized in PN signal based background calibration while large PN signal can be used for calibration to speed up the convergence process. Only two comparators and a digital adder are needed to achieve the adjustment. This technique can be applied to pipelined ADC with PN signal based background calibration.

REFERENCES

[1] H. Balasubramaniam, K. Hofmann, A 10 bit, 1.5b/stage pipeline ADC using a fully differential current conveyor with foreground calibration, IEEE Signals, Circuits and Systems (ISSCS), 2011, 1-4

[2] Ruitao Zhang, Jinshan Yu, Zhengping Zhang, Yonglu Wang, Zhu Can, Yu Zhou, Linearity improvement base on digital foreground calibration algorithm for a ultra high-speed analog-to-digital converter, IEEE Anti-Counterfeiting Security and Identification in Communication (ASID), 2010, 130-133.
[3] H. Adel, M. Dessouky, M. Louerat, H. Gicquel, H. Haddara, Foreground digital calibration of non-linear errors in pipelined A/D converters, IEEE Circuits and Systems (ISCAS), 2010, 569-572.
[4] C. R. Grace, P. J. Hurst, S. H. Lewis, A 12-bit 80-Msample/s pipelined ADC with bootstrapped digital calibration, IEEE J. of Solid-State Circuits, (40)2005, No. 5, 1038-1046.
[5] J. P. Keane, P. J. Hurst, S. H. Lewis, Background interstage gain calibration technique for pipelined ADCs, IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., (52)2005, No. 1, 32–43.
[6] Jun Ming, S.H. Lewis, An 8-bit 80-Msample/s pipelined analog-to-digital converter with background calibration, IEEE J. Solid-State Circuits, (36)2001, 1489-1497.
[7] Haoyue Wang, Xiaoyue Wang, Hurst, P.J, Lewis, S.H. Nested Digital Background Calibration of a 12-bit Pipelined ADC Without an Input SHA, IEEE J. Solid-State Circuits, (44)2009, No. 10, 2780-2789.
[8] H. C. Liu, Z. M. Lee, J.T. Wu, A 15-b 40-MS/s CMOS pipelined analog-to-digital converter with digital background calibration, IEEE J. Solid-State Circuits, (40)2005, No. 5 1047-1056.
[9] Jie Yuan, N.H. Farhat, J. Van der Spiegel, Background Calibration With Piecewise Linearized Error Model for CMOS Pipeline A/D Converter, IEEE Circuits and Systems I: Regular Papers, IEEE Transactions on, (55)2008, 311-321.
[10] T. Moosazadeh, M. Yavari, A novel digital background calibration technique for pipelined ADCs, IEEE Circuits and Systems for Communications (ECCSC), 2010, 127-130.

***Authors**: Associate Prof. Ning Ning, State Key Lab of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China, No.4, Section 2, North Jianshe Road, Chengdu, P. R. China, 610054, E-mail: ning_ning@uestc.edu.cn; Zhiling Sui, E-mail: ZhilingSui@gmail.com; Hua Chen, E-mail: chenhua009@126.com; Shuangheng Xu, E-mail: cshuanghx@163.com; Jun Zhang, E-mail: zhangjun_21@126.com; Jie Zheng, E-mail: 449617754@qq.com; Shuangyi Wu, E-mail: wsy979@gmail.com; Qi Yu, E-mail: qiyu@uestc.edu.cn.*