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A Dual Loop Control Strategy for Parallel Interleaved Three-Phase Four-Leg PWM Boost-Type Rectifier in UPS

Abstract. *This paper presents a dual-loop control strategy for parallel interleaved three-phase four-leg PWM boost-type rectifier in double conversion UPS. The interleaving method is adopted for its main benefit of harmonic cancellation. The current in the fourth leg is treated as a perturbation because the fourth leg is shared by rectifier and inverter, and the controller can be designed in a-b-c coordinate conveniently. The DC-bus voltage feedback in outer control loop can be delayed by quarter-cycle to filter out the oscillating component when the load of UPS is unbalanced. The performance of proposed control scheme is verified by experimental results.*

Streszczenie. *W artykule zaprezentowano strategię dwóch pętli sterowania trójfazowym czterogałęziowym prostownikiem PWM typu boost w układzie UPS. Wykorzystano metodę z przeplotem w celu eliminacji wpływu harmonicznych. (**Dwuobwodowa strategia sterowania trójfazowym prostownikiem PWM w układach UPS**)*

Keywords: Double conversion UPS; Interleaved four-leg PWM rectifier; Dual-loop controller; Instantaneous power.
Słowa kluczowe: układ ups, prostownik PWM, sterowanie z przeplotem

Introduction

UPS is being widely used to providing emergency power for critical loads. The double conversion UPS usually consists of a three-phase rectifier at the first stage and a three-phase inverter at the second stage. Compared with traditional three-phase diode rectifier and phase-controlled rectifier, PMW boost-type rectifier have advantages such as high power factor and low input harmonic distortion and is increasingly adopted as a high power quality solution in UPS [1]. In this paper, The UPS consists paralleling converters, for the reason that the interleaving method is an efficient way to reducing the harmonic currents and the size of passive components [2-4].

There have four kinds of topologies of PWM rectifier: 1) three-phase PWM rectifier with a reduced switch count [5], 2) three-phase three-leg PWM rectifier [6-9], 3) three-phase three-leg PWM rectifier with split DC-bus [10], 4) three-phase four-leg PWM rectifier [11]. Three-phase PWM rectifier with a reduced switch count is a low cost topology because the there are four switches in three-phase network. Three-phase three-leg PWM rectifier has been studied extensively for its high performance. However, if one of input is failed, the three-phase three-leg rectifier has to be changed into single-phase rectifier to maintaining the DC-bus. In this case, the output power of UPS would be reduced by two-third of rated power. Therefore, the three-phase four-wire PWM rectifier has gained more attention for the reason that zero sequence current can pass through an additional path. The remaining inputs of the four-leg rectifier can still be operating properly with two-third of rated power even if one of input is failed. Thus, output power of UPS can be doubled compared with the three-phase three-leg rectifier. Compared with rectifier with split DC-bus, the four-leg PWM rectifier is preferred because the capacitance of DC-bus capacitor can be smaller.

A dual-loop control scheme in a-b-c coordinate for four-leg PWM boost-type rectifier is presented in this paper. Thus, the three-phase input currents can be controlled independently. The current in fourth leg is treated as perturbation, therefore, the proportional-integral (PI) regulator in current inner loop is preferred to suppressing the perturbation compared with proportional (P) regulator. The front-end rectifier and back-end inverter share the fourth leg so that the UPS can be operating properly even if one of input is failed or the load is unbalanced. In condition the load is unbalanced, the inverter will absorb additional oscillating power whose frequency is double of fundamental frequency according to instantaneous power theory [12-16]. The DC-bus voltage will have the same oscillating component if the oscillating power is provided by DC-bus capacitor. The DC-bus voltage feedback in outer control loop can be delayed by quarter-cycle to gain a DC component for attenuating the impact on dual-loop controller caused by oscillating DC-bus voltage feedback. Thus, the four-leg PWM rectifier can operate properly even if the load of UPS is unbalanced. The control scheme is verified by experimental results.

Power flow of the UPS

Fig.1 shows the main circuit of the double conversion transformerless UPS. The rectifier and inverter in UPS share the fourth leg because the additional leg is necessary for both of them. If one of input is failed or the load is unbalanced, the zero sequence current will pass through the common leg. For the sake of simplicity in the analysis of power flow, the harmonic components in the UPS system is neglected. According to instantaneous power theory, the instantaneous power in the input of the UPS system is defined as

$$p_{in} = u_{sa} i_a + u_{sb} i_b + u_{sc} i_c \tag{1}$$

The instantaneous power in the output of the UPS system is defined as

$$p_{out} = u_{AN} i_{oa} + u_{BN} i_{ob} + u_{CN} i_{oc} \tag{2}$$

The PWM rectifier will balance the three-phase input current with low harmonic distortion and achieve unity power factor. Thus, when the grid voltage is balanced, the energy transferred from power grid to UPS is constant according to equation (1). The energy absorbed by inverter is constant when the load is balanced according to equation (2). The constant power will flow through the UPS.

However, the four-leg inverter should maintain a balanced output voltage even if the load is unbalanced which leads to non-constant energy transfer. In such case, the instantaneous power absorbed by inverter contains average component and oscillating component.

In such case, there exist two different methods to balance the energy transfer of the UPS when the load is unbalanced. The first one is that, the rectifier will provide the total instantaneous power to the third stage. The DC-bus voltage will be stabilized by this method because it is still a snubber stage. Therefore, it is essential to adjust three-phase input currents to balancing the energy transfer. However, the three-phase input currents will not be balanced, and it is complicated to calculate the respective reference of three-phase input currents precisely.

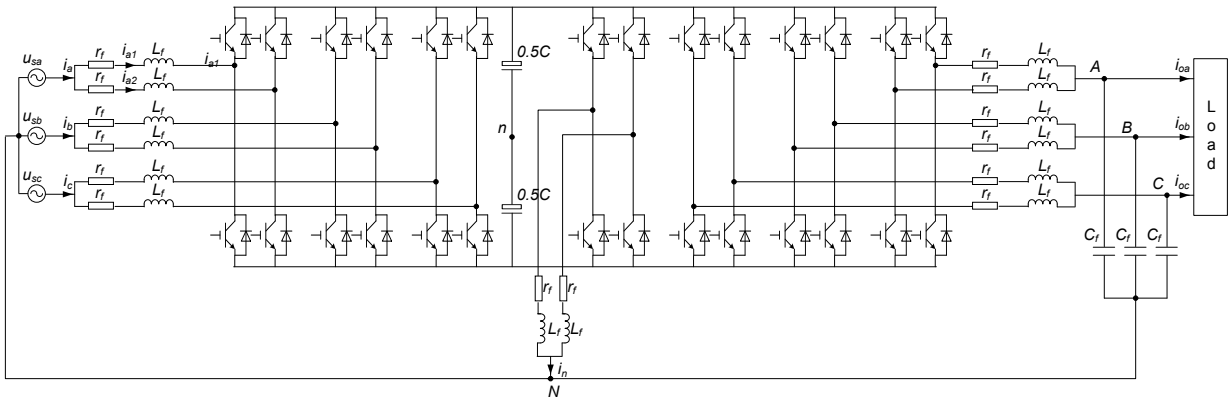


Fig.1. The main circuit of the UPS

The second method is that, the rectifier will provide the average power which means that the three-phase input currents can be balanced, but the DC-bus capacitor has to provide oscillating power. It means that DC-bus voltage will involve oscillating component. The oscillating DC-bus voltage will have considerable negative impact on the controller of rectifier.

Therefore, it is essential to decompose the DC-bus voltage into DC component and oscillating component for the aim of balancing the three-phase input current. Taking into consideration that the oscillating frequency is double of fundamental frequency and the amplitude of oscillating component is nearly constant. Thus, the oscillating component can be attenuated by delaying the DC-bus voltage of quarter cycle. Fig.2 shows the block diagram of quarter-cycle delay algorithm.

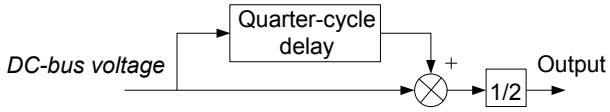


Fig.2. Block diagram of the quarter-cycle delay algorithm

Fig.3 shows the simulated waveforms of three-phase input currents when the load of UPS is unbalanced. In Fig.3(a), the three-phase input currents are distorted by the oscillating component of DC-bus voltage ($\pm$0.5V). In such case, the three-phase input currents involve additional low order harmonic components. In Fig.3(b), the quarter-cycle delay algorithm is adopted to achieve balanced input currents with low harmonic distortion.

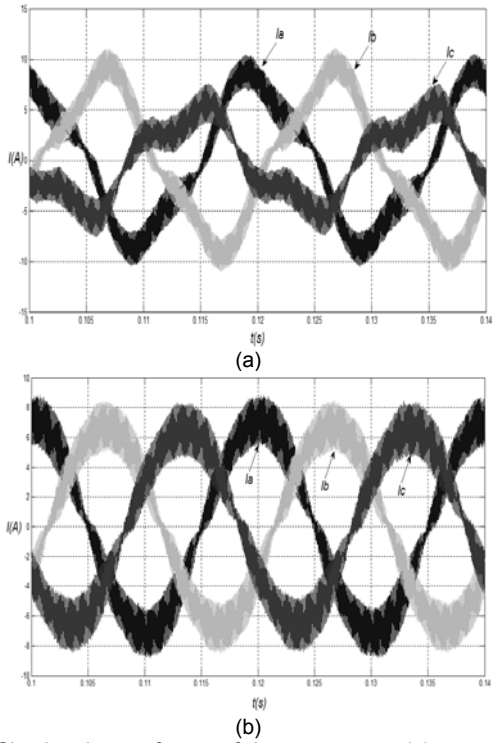


Fig.3. Simulated waveforms of input currents (a) quarter-cycle delay algorithm is not adopted (b) quarter-cycle delay algorithm is adopted

Interleaving method

For parallel three-phase voltage source converter (VSC), the parallel bridges in each phase can be used to suppressing current ripple with the interleaving method. It is an effective way for harmonic cancellation as it can help to reduce certain harmonics of current. The interleaving angle between with adjacent bridges is 2π/N, where N is the number of parallel bridges.

The sketch of current harmonic cancellation by interleaving method for two parallel bridges (a1,a2) is shown in Fig.4. The phase shift between carrier1 and carrier2 is π. PWM1 and PWM2 are switch vectors of the upper modules of phase a in each bridge. I_{a1} and I_{a2} are the inductor currents of phase a in each bridge, and I_a is the sum of I_{a1} and I_{a2} for a given phase. Only the high frequency current ripple components are shown in Fig.2. The ripple frequency of I_a is two times that of I_{a1} and I_{a2}, the ripple amplitude of I_a can be reduced. Therefore, the inductance of filter inductor in parallel interleaved VSC can be smaller than single VSC. For control loop, the transient response can be improved due to smaller inductance.

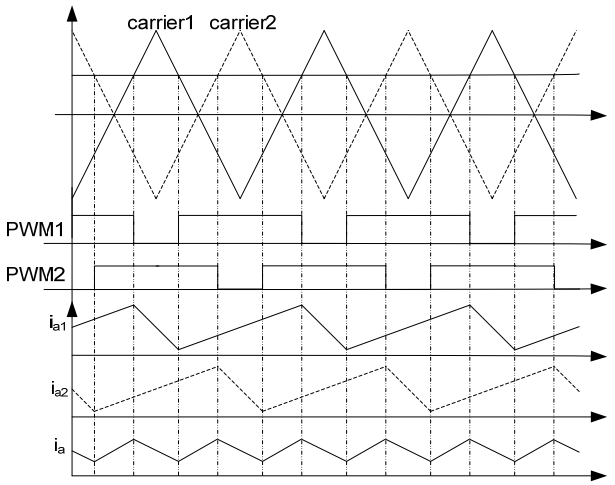


Fig.4. Sketch of interleaving method for the inductor current in bridge a1&a2

Characteristic of the four-leg PWM rectifier

The fourth leg is shared by rectifier and inverter, thus, the conventional approach of decomposing abc phase variables into stationary-frame αβo variables and then to synchronous-frame dqo variables will be complicated for the controller of four-leg PWM rectifier. The current in the fourth leg will exist when the three-phase inputs are unbalanced or the load is unbalanced. Taking into consideration the characteristics of the current in the fourth leg, it is convenient to treate the current as perturbation. The controller is adopted to attenuating the impact of current in fourth leg on rectifier.

The dual loop controller contains DC-bus voltage outer loop and inductor current inner loop. Typically, a PI regulator in the outer loop and a P regulator in the inner loop are incorporated. This controller has a good performance for three-phase three-leg PWM rectifier. However, for four-leg rectifier, the perturbation of the current in fourth leg will have a considerable negative impact on controller. Thus, The P regulator in inner loop will be replaced by PI regulator to achieve better performance. The phase lag at 50Hz caused by PI regulator in inner loop is small. Thus, it has a slight influence on the power factor of the rectifier.The key parameters of the system are listed in Table 1.

Table 1. Key parameters of the system

Parameters	Value
Input voltage: Ui	70.7V(rms)
Output voltage: Uo	70.7V(rms)
DC-bus voltage: Udc	250V
Filter inductor: Lf	1mH
ESR of inductor: rf	0.1Ω
Filter capacitor: Cf	150uF
DC-bus capacitor: C	12000uF
Switch frequency: fsw	8kHz
Sampling frequency: fsa	16kHz

Assuming the filer inductor in each phase is linear and neglecting the power loss of switch, the block diagram of control scheme for the rectifier is shown as Fig. 5.

Switching function S_x* (x=a,b,c,n) is defined as

$$(3)\quad \begin{cases} S_x^* = 1 & \text{upper switch close, lower switch open} \\ S_x^* = 0 & \text{upper switch open, lower switch close} \end{cases}$$

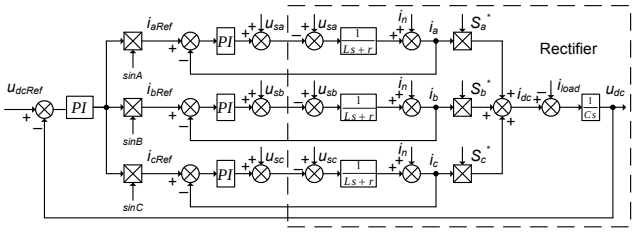


Fig.5. Block diagram of control scheme for the rectifier

The direct current control method is implemented on the rectifier because it shows good steay characteristic. The current controllers of the three-phase can be designed in the same way. Fig.6 shows the block diagram of control scheme for current inner loop of phase-a. K_p and K_i are parameters of the PI controller of inner loop, K_{pwm} is the PWM gain of the rectifier, and T_s is the sampling period. It is assumed that there exists half sampling period delay in the feed forward loop and one sampling period delay in the feedback loop. The equivalent inductance $L=L_f/2$, and the equivalent parasitic resistance $r=r_f/2$.

The open loop transfer function of the current loop is defined as

$$(4)\quad P(s) = \frac{K_{pwm}/r}{(0.5T_s s+1)[(L/r)s+1](T_s s+1)}$$

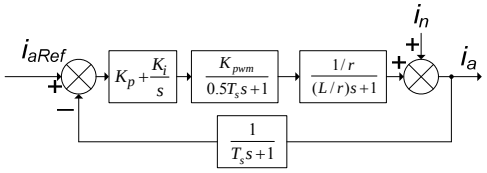


Fig.6. Block diagram of control scheme for current loop of phase-a

The design of PI controller can be done by following the designing approach, putting a zero at the frequency which can ensure 45° of phase margin at least and adjusting the gain to have the desired gain margin and bandwidth. According to the designing approach, the proportional coefficient K_p=13 and the integral coefficient K_i=23400. Fig.7 shows the bode diagram of current open loop. The phase margin is 45° and the open loop gain at 50Hz is 37.4dB, which means that the steady state error can be reduced effectively by the controller.

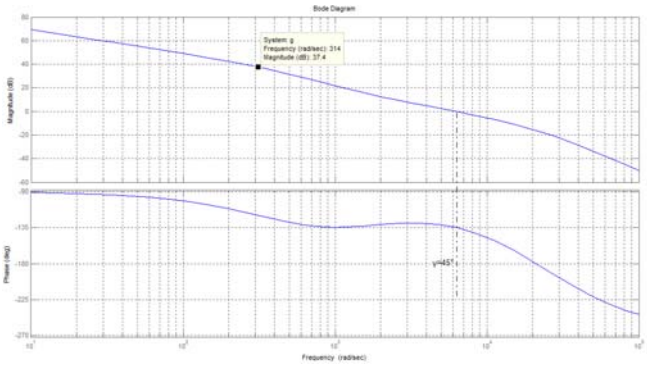


Fig.7. Bode digram of the current open loop

The tansfer function of the perturbation is given as

$$(5)\quad G_p(s) = \frac{s^3 + [(1.5T_s + T_L)/1.5T_sT_L]s^2 + 1/1.5T_sT_L s}{s^3 + [(1.5T_s + T_L)/1.5T_sT_L]s^2 + (1+K_p)/1.5T_sT_L s + K_i/1.5T_sT_L}$$

where $T_L = L/r$.

According to equation (5), the gain at 50Hz is -35.6dB, which means that the current loop can effectively suppress the perturbation of the current in fourth leg.

The current inner loop is equivalent to a first-oder inertia system for the purpose of designing the controller in outer loop conveniently, which is defined as

$$(6)\quad G_i'(s) = \frac{1}{T_i s + 1}$$

where $1/T_i$ is the cutting-off frequency of the current inner loop.

. The block diagram of control scheme for the DC-bus voltage outer loop is shown as

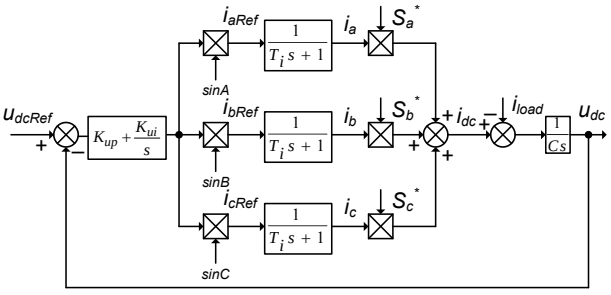


Fig.8. Block diagram of control scheme for the voltage loop

The DC-bus voltage outer loop can be equivalent to be a second-order system. According to the useful engineering design method [9], the proportional coefficient K_{up}=46.5, and integral coefficient K_{ui}=3418.

B. Modulation of the UPS

The 3-D space vector PWM(3-D SVPWM) is widely used in three-phase four-leg converters [17]. An convenient carrier-based PWM method which is proved to be equivalent to 3-D SVPWM was proposed [18].Therefore, the carrier-based PWM method with zero-sequence offset voltage is easier to implementing on the UPS. The fourth leg is shared by rectifier and inverter, thus, the pole voltage reference for common leg is given as [19]

$$V_{fn}^{*}=\begin{cases}-\dfrac{V_{\max}^{*}}{2}, & V_{\min}^{*}>0\\ -\dfrac{V_{\min}^{*}}{2}, & V_{\max}^{*}<0\\ -\dfrac{V_{\max}^{*}+V_{\min}^{*}}{2}, & \text{el se}\end{cases} \tag{7}$$

$$\begin{cases}V_{\max}^{*}=\max\left(V_{raf}^{*},V_{rbf}^{*},V_{rcf}^{*},V_{iaf}^{*},V_{ibf}^{*},V_{icf}^{*}\right)\\ V_{\min}^{*}=\min\left(V_{raf}^{*},V_{rbf}^{*},V_{rcf}^{*},V_{iaf}^{*},V_{ibf}^{*},V_{icf}^{*}\right)\end{cases} \tag{8}$$

where V^{*}_{raf}, V^{*}_{rbf} and V^{*}_{rcf} are three line to neutral input voltage references for rectifier. V^{*}_{iaf}, V^{*}_{ibf} and V^{*}_{icf} are three line to neutral output voltage references for inverter.

The respective pole voltage references for rectifier and inverter can be calculated as

$$\begin{cases}V_{ran}^{*}=V_{raf}^{*}+V_{fn}^{*}\\ V_{rbn}^{*}=V_{rbf}^{*}+V_{fn}^{*}\\ V_{rcn}^{*}=V_{rcf}^{*}+V_{fn}^{*}\end{cases} \tag{9}$$

$$\begin{cases}V_{ian}^{*}=V_{iaf}^{*}+V_{fn}^{*}\\ V_{ibn}^{*}=V_{ibf}^{*}+V_{fn}^{*}\\ V_{icn}^{*}=V_{icf}^{*}+V_{fn}^{*}\end{cases} \tag{10}$$

Experimental Results

The proposed control scheme has been evaluated on a 3kW prototype. The main control chips are DSP (TMS320F2812) and CPLD (EPM1270).

Fig.9 shows the high frequency current ripple waveforms of I_{a1}, I_{a2} and I_a. I_{a1} and I_{a2} are inductor currents of the parallel legs, and I_a is the sum of the two currents. The ripple amplitude of Ia is reduced, and the ripple frequency is doubled.

Fig.10 shows the experimental waveforms of three-phase input currents and DC-bus voltage when the output power of the prototype is with rated power (3kW). The DC-bus voltage is stable and the harmonic distortion of three-phase input currents is low. Fig.11 shows the experimental waveforms of three-phase currents and DC-bus voltage when the load is unbalanced (Phase a with 1kW load and the others with no-load). Oscillating component of DC-bus voltage is $\pm$0.6V. In Fig.11, degrees of unbalance for the three-phase input currents have been reduced effectively by the quarter-cycle delay algorithm. Compared with the simulated waveform in Fig.3(b), the harmonic distortion of three-phase input currents is higher because the oscillating component can not be cancelled completely due to sampling error and harmonics.

Fig.12 shows the waveforms of the input currents when one of inputs is failed. In Fig.12, the other two inputs are operating properly when phase c is failed. The input power of the four-leg rectifier has been reduced by 1/3. It has been proved that the three-phase currents of rectifier can be controlled independently.

Conclusion

This paper presents a dual loop control strategy in a-b-c coordinate for parallel interleaved three-phase four-leg PWM boost-type rectifier in double conversion transformer-less UPS. The use of interleaving for the UPS has the merit of harmonic cancellation. With the proposed control scheme, if one of input is failed, the remaining inputs can still be operating properly. According to instantaneous power theory, the DC-bus capacitor has to provide oscillating power when the load is unbalanced so as to maintain a constant input power. The quarter-cycle delay algorithm can attenuate the negative impact on controller caused by oscillating voltage of DC-bus. Theoretical predictions are in close agreement with experimental results.

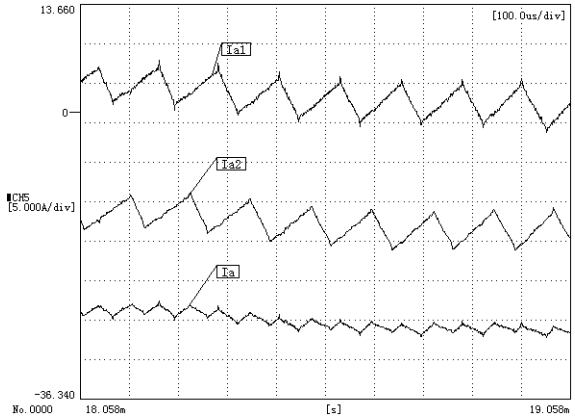


Fig.9. Current waveforms of phase-a of rectifier

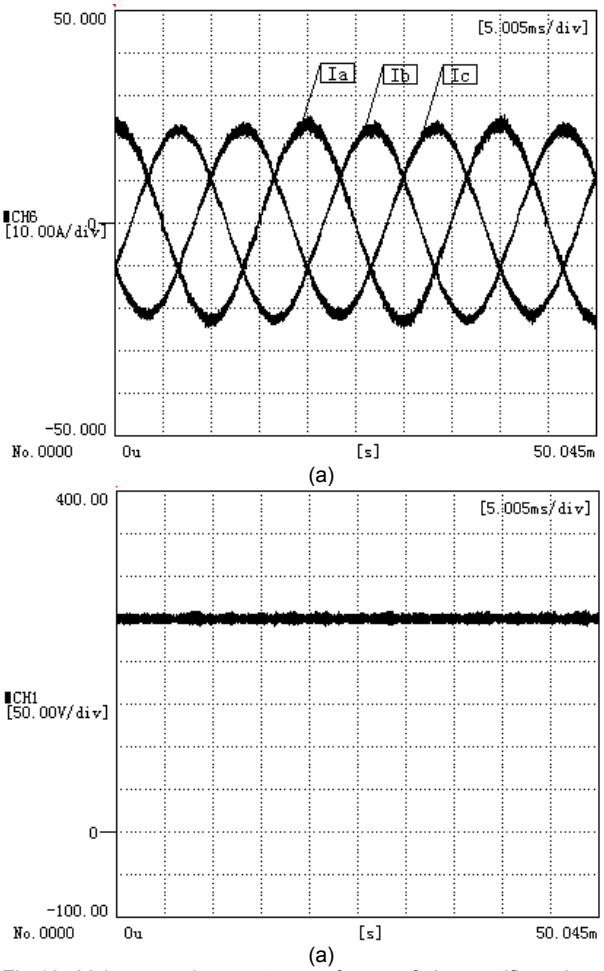
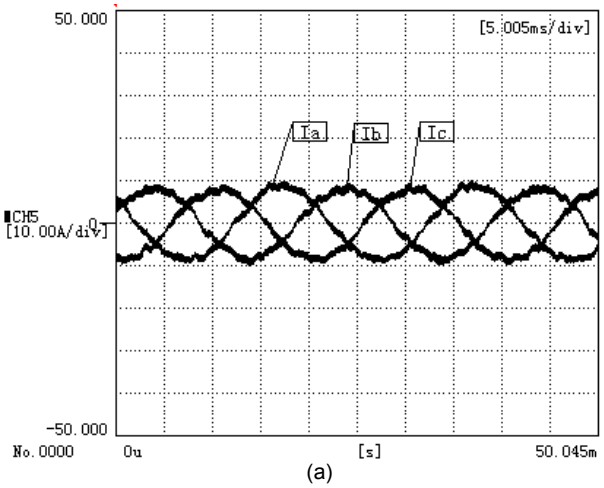
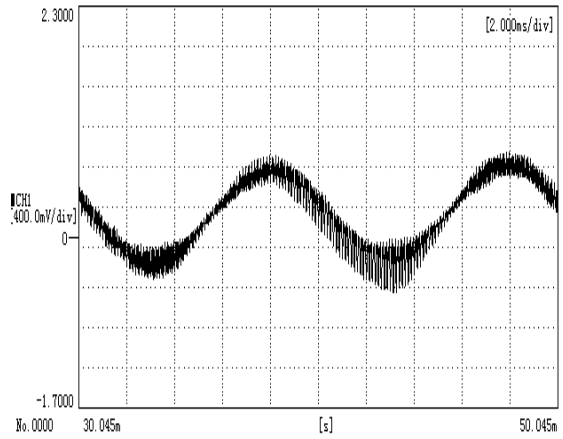


Fig.10. Voltage and current waveforms of the rectifier when the load is balanced (3kW): (a) input currents (b) DC-bus voltage



(a)



(b)

Fig.11. Voltage and current waveforms of the rectifier when the load is unbalanced (1kW) (a) input currents (b) Oscillating component of DC-bus voltage

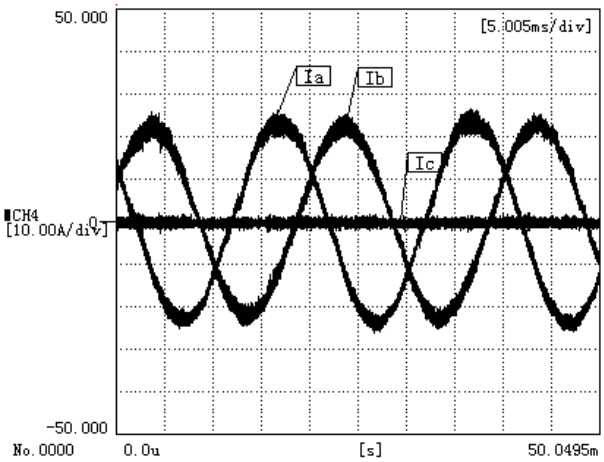


Fig.12. Current waveforms of the rectifier when one of inputs is failed

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