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Parametric fault detection in analog circuits containing MOS transistors

***Abstract**. In this paper, algorithm for parametric fault diagnosis of nonlinear, analog circuits containing MOS is presented. This method applies power supply current waveform IDD as an indicator of a device feature. Test signal is filtered using a discrete wavelet transform filter bank to obtain signal sensitive to changes of device parameters. Coefficients of the polynomial approximating the component are calculated and used to formulate a learning vector of a feedforward neural network. Thus, it is possible to achieve data compression without the considerable loss of information about the tested device. An illustrative numerical example is presented.*

***Streszczenie.** W pracy przedstawiono metodę wykrywania uszkodzeń parametrycznych w układach analogowych zawierających tranzystory MOS. W zastosowanym algorytmie informacje o właściwościach układu są zakodowane w przebiegu prądu źródła, zasilającego obwód w stanie nieustalonym. Sygnał testowy jest filtrowany, by uwypuklić właściwości układu. Aby zachować istotę informacji o układzie, jako wektory uczące sieć neuronową zastosowano współczynniki wielomianów aproksymujących wybrany składnik sygnału testowego. Działanie algorytmu zilustrowano na praktycznym przykładzie. (**Wykrywanie uszkodzeń parametrycznych w układach analogowych zawierających tranzystory MOS**)*

Keywords: analog circuits, fault detection, discrete wavelet transform, feedforward neural network
Słowa kluczowe: układy analogowe, wykrywanie uszkodzeń, dyskretna transformacja falkowa, jednokierunkowe sieci neuronowe.

Introduction

Faults location and detection in electronic equipment is one of the fundamental problems in production of reliable and safe electronic, multi-element systems. For diagnosis of faults in numerical electronic devices some effective and automatic procedures have been worked out. Unfortunately, diagnoses of analog circuits are mainly based on engineers' experience, since no universal and reliable techniques have been determined so far.

The review of papers dealing with diagnosis problem [1], [2] shows that two basic types of faults: catastrophic and parametric are discussed. In case of catastrophic faults, which rely on short or open circuit, we deal with the problem of the change of circuit topology. Failures, in which there is no change of circuit topology, and only values of parameters change, are called parametric faults. Both types of faults may cause improper functioning or even destruction of the system, therefore the precise fault diagnosis of the produced electrical devices is essential.

Monitoring of supply current (test IDDQ), a method introduced in the early nineties of the last century, is an effective diagnosis approach of digital CMOS [3], [4]. In order to overcome some limitations of this method, tracing of supply current in unsteady state, caused by a shock change of supply voltage [5], [6], [7] was applied (test IDD). The IDD transient response method performs a dynamic measurement of the power supply current when VDD is changed from a nominal value to a half of nominal value. Achievements, which this method brought to diagnostic investigations of digital devices, caused its usage also for analog circuits testing [8], [9]. Yet a great changeability of such circuits makes their diagnosis difficult and requires further studies.

In the middle of the nineties, some papers were published in which neural networks were applied for processing of data, obtained as a result of circuit testing. This application improved the diagnosis process [11], [12], [13]. It seems that the excellent ability of classification of artificial neural network, applied in an appropriate way, can be effectively used for detecting possible faults in analog circuits. However, the research shows that the use of such procedures requires additional operation adjusting data obtained from the measurements made during the tests. It was found that samples of the measured current constituted too large data set to be introduced to the net. Therefore, bringing preliminary processing in which data has to be compressed and additionally has to emphasize a distinguishing feature, became necessary. Paper [14] shows that both tasks for preliminary procedures are well performed by a wavelet transformation.

The aim of the conducted research was to test if transient supply current IDD may be useful in parametric fault detection in analog circuits containing MOS transistors.

Test signals measurement

The detection of parametric faults is more difficult than in case of catastrophic faults, because the changes in the circuit are less radical. Therefore, the method of testing must be more sensitive than in recognition of the catastrophic fault. It should be planned to obtain signals sensitive for changes in parameters within established limits. The test results should contain as much information as possible about dynamic features of the tested circuits.

In some cases transient supply current IDD may not contain enough information for detecting parametric faults. Therefore, all available signals in the existing circuit outputs should be used. In more difficult instances creation of special outputs for tests may be essential.

Additionally, to stimulate oscillations of the supply current during the test, one should use extra components (eg. coils and capacitors), connected to external terminals [15]. Due to such a procedure, a test signal contains more information about the circuit.

Test signals preprocessing

In order to exposure changes of features of the device, resulting from modification of parameters, test signals (transient supply currents IDD) are divided into elements by means of bank of filters formed with the use of discrete wavelet transformations. The wavelet with scale a and shifting b is the function given by the equation:

$$\psi_{ab}(t) = \frac{1}{\sqrt{a}}\psi\left(\frac{t-b}{a}\right), \tag{1}$$

where ψ represents the basic wavelet, i.e., function determining type of the used wavelet transformation. Assuming

$$a = 2^m \quad \text{and} \quad b = n2^m$$

we have the equation

(2) $$\psi_{nm}(t) = 2^{-\frac{m}{2}}\psi\left(2^{-m}\left(t - n2^{m}\right)\right)$$

where m and n are natural numbers, determining the packet of wavelets being the basis of discrete wavelet transformation.

Each of these mentioned functions appoints the pair of complementary filters, which divide the signal into two parts: the lower part of frequency band, i.e., *approximation* and the upper part of frequency band, i.e., *details*. The approximations are the high-scale, low-frequency components of the signal. The details are the low-scale, high-frequency components. The filtering process, at its most basic level, is shown below in the figure 1

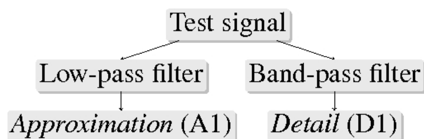

Fig.1. Division of a test signal into approximation and detal

The decomposition process can be iterated, so that one signal is broken down into many components. This task is performed by some filters constituting a complementary set. Such filters, and a five level division of the signal is illustrated by decomposition tree given in the figure 2.

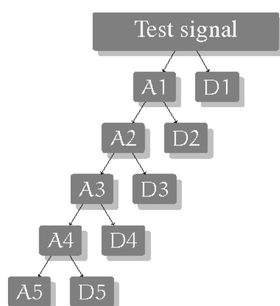

Fig.2. Example signal's wavelet decomposition tree

After dividing test signals into elements, one of them is used in diagnosis process. The chosen element should show the biggest sensitivity and also regularity over the change in value of device parameter.

Neural network

It is assumed that an artificial *feedforward neural network* is an algorithm, and its basic component, called neuron, erforms calculations given by the equation:

(3) $$y = f\left(\sum_{i=0}^{lw} w_i x_i\right),$$

where numbers $x_0, x_1, \ldots, x_{lw}$ make input signal $w_0, w_1, \ldots, w_{lw}$ are weight, modified at learning process, lw determines number of neuron inputs, $f(*)$ is a function, called *neuron activation function*, and y is an output signal.

Neurons are arranged in layers. The first one, called *an input layer* is exceptional since it has no neurons, only input signals. The following layers, called *hidden*, contain neurons sending their own output signals to all neurons of the following layer. The last layer, called the output, produces the output signals of the whole network.

Input vectors of the neural network, used for learning to recognize the parametric fault, are made in the following way: At the beginning, test signals are determined for different values of the tested components. These values of parameter of the chosen component are modified to cover evenly the whole range of changes, which should be taken into account. Next, using a wavelet filter bank, the tested signals are divided into elements. The most precise element, showing regular changes together with the change of the parameter, is chosen.

Each signal obtained in such way contains information about properties of the tested device. Nevertheless, samples of the chosen component (approximation or detail) of power supply current waveform IDD can not be used as input signals of neural network, because there are too many of them. Compression of data is required. It can be achieved by reducing the number of samples in signals, to obtain the proper size of vector. However this method causes the loss of information. To prevent this adverse phenomenon, an approximating polynomial $s_a(t)$ of the signal $s(t)$ that has been sampled at $t_0, t_1, \ldots, t_k$

(4) $$s = \left[s_1(t_1) \quad s_2(t_2) \quad \cdots \quad s_k(t_k)\right]^T,$$

is determined. Its coefficients make the neural network input vector x.

Creation of input vectors

We compute coefficients $x_0, x_1, \ldots, x_{lw}$ of an approximating polynomial $s_a(t)$ of degree n, given by equation

(5) $$s_a(t_i) = x_0 + x_1\,t_i + x_2\,t_i^2 + \cdots + x_n\,t_i^n = \\ = \begin{bmatrix}1 & t_i & \cdots & t_i^n\end{bmatrix}\begin{bmatrix}x_0 \\ x_1 \\ \cdots \\ x_n\end{bmatrix}$$

where the value t_i *(i=1,2,3,...,k)* determines the sample $s_a(t_i)$.

Writing down equation 5 for all k samples in matrix form we obtain

(6) $$\begin{bmatrix}s_a(t_1) \\ s_a(t_2) \\ \cdots \\ s_a(t_k)\end{bmatrix} = \begin{bmatrix}1 & t_1 & \cdots & t_1^n \\ 1 & t_2 & \cdots & t_2^n \\ \cdots & \cdots & \cdots & \cdots \\ 1 & t_k & \cdots & t_k^n\end{bmatrix}\begin{bmatrix}x_0 \\ x_1 \\ \cdots \\ x_n\end{bmatrix}$$

which given in more compact form can be written as follows:

(7) $$s_a = Ax.$$

Values of an approximating polynomial are the nearest to samples of test signal, when the expression

$$|| s - s_a ||$$

takes a minimal value. It takes place when the vector s_a is determined by approximating polynomial whose coefficients x are calculated from the equation

(8) $$x = A^{+} s_a$$

in which A^{+} determines Moore–Penrose pseudoinverse of a matrix A .

If approximation is proper, then coefficients x of approximating polynomial represent the whole data involved in the signal. Then x can be taken as an input signal to neural network.

Example

The circuit, shown in the figure 3, set an example. In order to enlarge sensitivity of the test signals for change of circuit parameters, one coil has been mounted in series with power source.

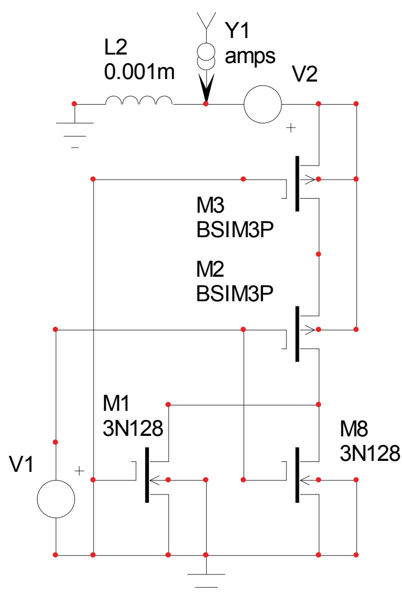

Fig. 3. The test circuit

To measure of the transient supply current we need to set the tested circuit in an unsteady state. For this purpose the VDD value was changed from the nominal value (5V) to value equal 2V like step function.

Mistakes in fabrication of electronic devices provoke changes of model parameters applied in computer symulation. Therefore changes of model parameters are treated as parametric faults in this investigation. The circuit response was calculated using ICAP4 simulator with employing BSIM3P PMOS Level=8 for M2 and M3, and _M1_mod NMOS Level=1 for M1 and M8 transistors. All nominal values of model parameter are shown in the Tabs 1 and 2.

As an example neural network learned to recognize changes value of parameter K1 (bulk effect coefficent) in the circuit, shown in the figure 3 is presented. The application in learning process of test signals coming from the circuits, whose model parameters change within tolerance limits, enable to consider variations of components occurring in practice.

Table 1. Parameters of BSIM3P model

Name	Value	Name	Value
K1	.8362093	UB	1.E-19
K2	-8.60662E-02	UC	-2.73E-11
K3	1.82	VSAT	103503.2
K3B	-0.24	A0	.4716551
W0	2.1E-6	AGS	0.12
NLX	1.28E-8	KETA	-1.871516E-03
DVT0W	0.232	A1	.3417965
DVT1W	4.5E6	A2	0.83
DVT2W	-0.0023	RDSW	460
DVT0	1.903801	PRWG	-0.001
DVT1	.5333922	PRWB	-0.323
DVT2	-.1862677	WINT	1.22E-7
U0	138.7609	LINT	6.23E-8
UA	1.39995E-09	VOFF	-.074182
-	-	NFACTOR	1.54389

Table 2. Parameters of BSIM3P model

Name	Value	Name	Value
NFACTOR	1.54389	AT	33000
ETA0	6.024776E-02	TNOM	27.0
ETAB	-4.64593E-03	PRT	64.5
DSUB	.23222404	UTE	-1.5
CIT	-1.015667E-03	KT1	-0.25
CDSC	8.937517E-04	KT1L	0
CDSCD	1.04E-4	KT2	-0.032
CDSCB	1.45E-4	UA1	4.312E-9
PCLM	.989	UB1	6.65E-19
PDIBLC1	2.07418E-02	UC1	0
PDIBLC2	1.33813E-3	TOX	9,00E-09
DROUT	.3222404	XJ	1.00000E-07
PSCBE1	118000	NCH	3.533024E+17
PSCBE2	1,00E-09	VTH0	-.6732829

The values of parameter K1 selected for creation of learning vectors are given in the table 3. The nominal value of K1 is 0.8362093.

Table 3.

The values of parameter K1	
0.43	1.43
nominal value	1.83
1.03	2.03

The process of decomposition of test signal (IDD) was made according to the scheme given on the figure 2. To calculate wavelet transformation, the wavelet db10 was used. In the presented example, the detail at level 9 of power supply current waveform, shown in the figure 4, appeared to be a signal meeting criteria given above. A polynomials of degree 6 were used to approximate selected components of the test signals to obtain learning vectors.

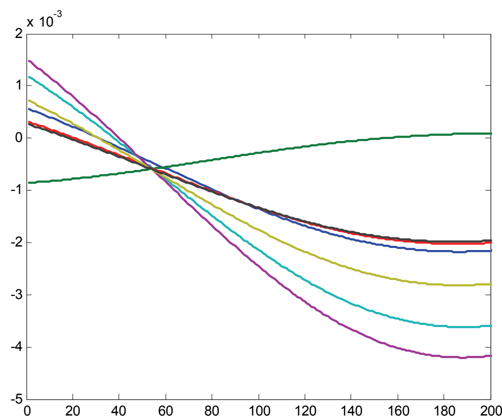

Fig. 4. Components (D9) of the test signas for different values of parameter K1 presented in the table 3

A neural network, with neurons having sigmoidal activation functions in two hidden layers, was applied. In the output layer linear activation functions were used. The structure of the neural network, shown on the figure 5, was created in heuristic way, taking to account neuron number minimization and its ability to generalize.

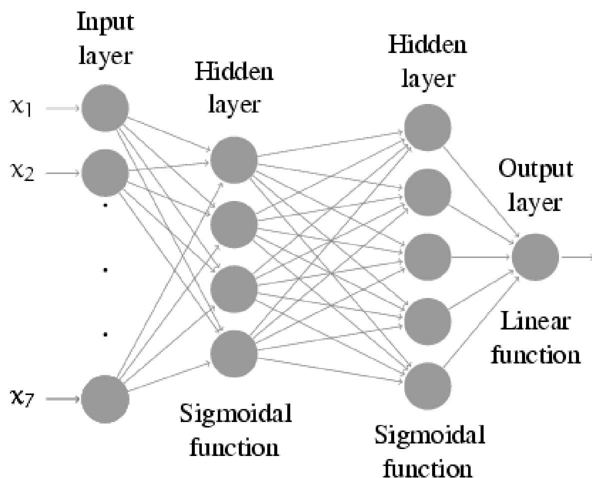

Fig.5. Neural network

Table 4 includes the checking results of the neural network working in the described case. All tests which were conducted showed the effectiveness of the given algorithm.

Table 4. The values of parameter K1

Assumed	From NN
0. 8362093	8.2963e-001
1.0362093	1.0309e+000
1.2362093	1.2456e+000
1.4362093	1.4328e+000
1.6362093	1.6160e+000
1.9362093	1.9280e+000

Conclusions

To sum up, the proposed algorithm enables a correct recognition of single parametric defects in circuit containing MOS transistors. However, test conditions and preprocessing proces should to generate learning signals sensitive to changes of the chosen parameter. Therefore, there is the necessity to formulate an individual project of test conditions for a given device and a given parameter. Secondly, creation of the learning vectors, with coefficients of approximating polynomial adequate element IDD, allowed a considerable compression of data without the loss of information concerning the circuit. Consequently, learning of a neural network is precise.

Finally, the conducted tests show that the size of the constructed network should be established in such a manner that the number of neurons is sufficient to remember the input information, and at the same time the neural network is able to generalize.

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