Stanisław HAŁGAS, Michał TADEUSIEWICZ

Faculty of Electrical, Electronic, Computer and Control Engineering, Technical University of Lodz

Analysis of CMOS circuits having multiple DC operating points

Abstract. *This paper is devoted to the analysis of the circuits containing short-channel MOS transistors, having multiple DC solutions (operating points). The transistors are characterized by the PSP model, the most advanced surface-potential-based compact MOSFET model, selected (since December 2005) as standard for the new generation of integrated circuits. This paper offers an algorithm enabling us to find multiple DC solutions and trace multivalued input-output characteristics of integrated circuits using the latest PSP 103.1.1 MOSFET model. The main idea of the algorithm is based on a single-valued driving point characteristic, called a test characteristic and the section-wise piecewise-linear approximations. The approach proposed in this paper is illustrated via a numerical example.*

Streszczenie. *Praca dotyczy analizy układów zawierających tranzystory MOS z krótkim kanałem, mających wiele rozwiązań DC. Tranzystory są opisane za pomocą modelu PSP, najbardziej zaawansowanego, opartego na koncepcji potencjału powierzchniowego modelu MOSFET, uznanego w 2005 roku za standardowy w zastosowaniu do nowej generacji układów scalonych. W pracy zaproponowano algorytm obliczania wielokrotnych rozwiązań DC oraz wyznaczania wielowartościowych charakterystyk typu wejście-wyjście układów scalonych, z użyciem najnowszej wersji PSP 103.1.1 modelu MOSFET. W algorytmie wykorzystano pewne jedno-wartościowe charakterystyki wejściowe, zwane charakterystykami testowymi oraz uogólnioną odcinkowo-liniową aproksymację. Dla ilustracji podano przykład liczbowy. (**Analiza układów CMOS o wielu rozwiązaniach DC**)*

Keywords: CMOS circuits, DC analysis, multiple solutions, transfer characteristics.
Słowa kluczowe: analiza stałoprądowa, charakterystyki przejściowe, rozwiązania wielokrotne, układy CMOS.

Introduction

Circuits having multiple DC solutions play an important role in electronics. The basic questions of the analysis and design of this class of circuits are finding all the solutions and tracing input-output characteristics. Numerous methods have been proposed for tackling these problems over the last few decades. Unfortunately, the proposed methods are very time-consuming and enable us to consider only small-sized circuits.

Among various approaches to finding all the DC solutions the simplest and the most commonly used are based on piecewise-linear approximations and computation techniques [1]-[9]. Only a few methods refer to the circuits described by smooth nonlinearities [10]-[14]. They are much more complex and difficult for implementation. Several concepts have been developed in this area based on the contraction method, the Newton homotopy, interval analysis, the simplex method and partitioning of the circuit in subcircuits. The idea of successive contraction, division and elimination of some hyperrectangular regions, where the solutions are sought is very useful and enables us to analyse both piecewise-linear and smooth circuits [4], [14].

Input-output characteristics are necessary to accomplish some design objective of nonlinear circuits. If a circuit has multiple DC solutions, the characteristics are not necessarily single-valued functions of the independent variables. Unlike single-valued, the multi-valued characteristics are very difficult to trace. There are several methods for computing the multi-valued input-output characteristics, e.g. [15]-[17]. Most of them are based on piecewise-linear approximation of nonlinear functions. Others suffer from major shortcomings due to the sharp-turning-point problem. Thus, the problem of tracing multi-valued characteristics is still open.

Most of the papers relating to the discussed above problems concentrate on the circuits containing bipolar transistors. The transistors are characterized by the Ebers-Moll or the Gummel-Poon model, including small number of nonlinear elements and parameters. The circuits have compact mathematical representation which makes possible to perform both qualitative and quantitative analysis. In contemporary electronics the CMOS circuits dominate the bipolar ones. A short-channel MOS transistor made in nanometer process has very complicated model described by hundreds of nonlinear equations and huge number of parameters. In such a case a different approach to the analysis is necessary. Since December 2005 the most advanced surface-potential-based compact MOSFET model was selected as standard for the new generation of integrated circuits [18]-[19], called the PSP model. In December 2009, PSP 103.1.1 model was released.

This paper offers for the first time an algorithm for finding the multiple DC solutions and the input-output characteristics of integrated CMOS circuits using the latest PSP 103.1.1 MOSFET model

Finding the multiple DC solutions and the input-output characteristics

Let us consider a CMOS circuit having multiple DC solutions, where the MOSFETs are characterised by the PSP 103.1.1 model. To find the multiple solutions we choose a test node, connect to this node a voltage source and trace the characteristic $i = f(v)$ (see Fig.1).

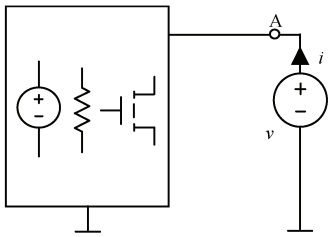

Fig.1. Circuit for tracing the test characteristic $i = f(v)$

We assume that the characteristic is single-valued and call it a test characteristic [13], [17]. Then we determine the values of v corresponding to $i = 0$. For each of these values the circuit shown in Fig. 1 is the same as the original circuit. To compute the test characteristic we apply the step-by–step method for succeeding values of v, every time using the node approach and the Newton-Raphson algorithm. Selecting the values of the node voltages corresponding to $i = 0$ we obtain the multiple DC solutions. Similarly we trace an input-output characteristic. If this characteristic expresses the output voltage in terms of the input voltage $v_{out} = g(v_{in})$, we choose discrete values of $v_{in} \in \{v_{in}^{(0)}, v_{in}^{(1)}, \ldots, v_{in}^{(M)}\}$ and for each of the values trace the test characteristic (see Fig. 2). Next we find all the values of v_{out} for each value of v corresponding to $i = 0$.

As a result we obtain one or several values of v_{out} at the given $v_{in}^{(j)}$, $j=1,\ldots,M$. They are considered as the points of the characteristic $v_{out}=g(v_{in})$ at $v_{in}^{(j)}$.

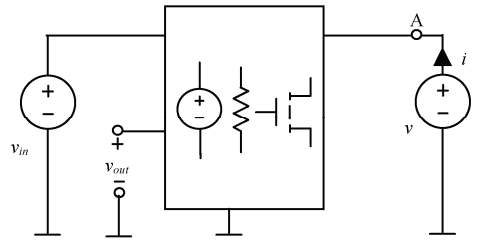

Fig. 2. Circuit illustrating the procedure for tracing the characteristic $v_{out}=g(v_{in})$

Mathematical representation of the circuits containing the PSP modelled transistors

The described above method operates on original equations of the PSP model. Therefore at each step of the algorithm hundreds of nonlinear equations describing a single MOS transistor have to be considered to obtain the drain, bulk, source and gate currents in terms of the external voltages of the transistor. Moreover, since most of the transistor parameters scale with geometry, a local parameter set has to be generated first. Thus, the process is very time consuming and makes possible to analyse only rather small-scale circuits. To overcome this drawback we use a closed form analytical formula for representing scalar functions of *n* variables, called a section–wise piecewise–linear representation (SPLR), proposed by Chua and Kang [20]. The coefficients of the representation can be easily computed using the formulae given in [20]. Some of them are repeated below. In CMOS transistor circuits we operate with the DC terminal currents being continuous functions of three (or two in the case when $v_{sb}=0$) voltages: v_{gs}, v_{ds} and v_{sb}.

Let us consider a special case of the SPLR representation relating to a continuous, single–valued function of two variables $f(x_1,x_2)$. We assume that a sufficient number of data points has been selected so that the function can be effectively approximated by a piecewise-linear function of a single variable, over every cross section obtained by freezing any variable. The function $f(x_1,x_2)$ can be described by the following section–wise piecewise–linear canonical representation [20]

$$f(x_1,x_2)= = a_0(x_2)+a_1(x_2)\,x_1+\sum_{j=1}^{N}\left(b_j(x_2)\left|x_1-x_1^{(j)}(x_2)\right|\right), \tag{1}$$

where: N is the number of breakpoints of the corresponding piecewise-linear function of a single variable over every cross section obtained by freezing the variable x_2, $x_1^{(j)}(x_2)$ $j=1,\ldots,N$ are piecewise-linear functions expressing the variables $x_1^{(j)}$ in terms of x_2,

$$a_1(x_2)=\frac{1}{2}\left(m_0(x_2)+m_N(x_2)\right), \tag{2}$$

$$b_j(x_2)=\frac{1}{2}\left(m_j(x_2)-m_{j-1}(x_2)\right),\quad j=1,\ldots,N, \tag{3}$$

$m_j\left(x_2^{(i)}\right)$ $i=1,\ldots,M$, $j=0,\ldots,N$ are the slopes of the segments of piecewise-linear functions $f\left(x_1,x_2^{(i)}\right)$, and

$$a_0(x_2)=f(0,x_2)-\sum_{j=1}^{N}\left(b_j(x_2)\left|x_1^{(j)}(x_2)\right|\right). \tag{4}$$

Equation (1) contains $2N+2$ functions of one variable x_2: $a_0(x_2),\ a_1(x_2), b_j(x_2), x_1^{(j)}(x_2),\ j=1,\cdots,N$ which are described by the standard piecewise–linear canonical representation.

The analysis of CMOS circuits made in nanometer technology is carried out as follows. At first the families of DC characteristics: $i_d=\hat{i}_d(v_{gs},v_{ds},v_{sb})$, $i_s=\hat{i}_s(v_{gs},v_{ds},v_{sb})$, $i_b=\hat{i}_b(v_{gs},v_{ds},v_{sb})$ and $i_g=\hat{i}_g(v_{gs},v_{ds},v_{sb})$ of transistors are computed using PSP103.1.1 model. Next the corresponding section–wise piecewise–linear functions are created and the corresponding controlled current sources are introduced into the circuits. Finally, the node equations of the circuit are formulated and the appropriate procedure of finding the multiple DC solutions or the input-output characteristics is applied.

The approach described in this paper was implemented in computer program using Delphi and tested using several CMOS circuits made in nanometer technology. The computations were executed on PC Pentium Core 2 Duo E6400.

Example

Let us consider the circuit shown in Fig. 3 [21] – [22], containing 10 MOS transistors made in 100nm process. The W/L values of the transistors are indicated in the figure. Using the proposed approach with $N=13$ we form SPLR for each MOS transistor with a specific geometry.

We wish to find the multiple DC solutions for $v_{in}=0.5\,\mathrm{V}$ and the input-output characteristic $v_{out}=g(v_{in})$ of the circuit depicted in Fig. 3. For this purpose we trace the test characteristic $i=f(v)$ at the node A (see Fig. 4) using the node approach and the Newton-Raphson algorithm. The test characteristic leads to 3 DC solutions:

v^{*} = [0.500 0.088 0.500 0.994 0.088 0.002 1.000 0.002 0.002 1.000 0.500 0.912 0.500 0.006 0.006 0.998 0.000 0.998 0.998 0.000]$^{\mathrm{T}}$,

v^{**} = [0.500 0.088 0.500 0.994 0.088 0.528 0.511 0.528 0.528 0.511 0.500 0.912 0.500 0.006 0.006 0.472 0.489 0.472 0.472 0.489]$^{\mathrm{T}}$,

v^{***} = [0.500 0.088 0.500 0.994 0.088 1.000 0.000 1.000 1.000 0.000 0.500 0.912 0.500 0.006 0.006 0.000 1.000 0.000 0.000 1.000]$^{\mathrm{T}}$.

The time consumed by the method is 1.3s. Using unprocessed PSP 103.1.1 model of the MOS transistors, represented by hundreds of nonlinear equations, we obtain very similar solutions in 47s. To find the input-output characteristic $v_{out}=g(v_{in})$ we repeat the described procedure for different values of $v_{in}\in[0,1]\,\mathrm{V}$ with the step equals 0.02V. The characteristic is shown in Fig. 5. The time consumed by the method is 141s. The obtained characteristic is almost identical as the one found on the basis of the original PSP model.

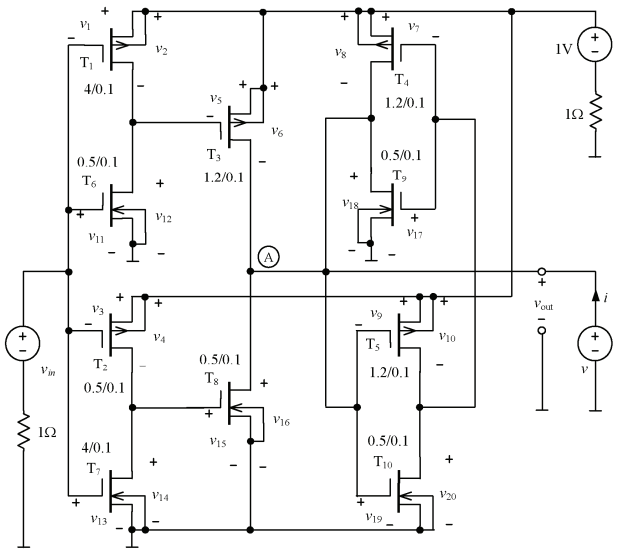

Fig. 3. An exemplary circuit

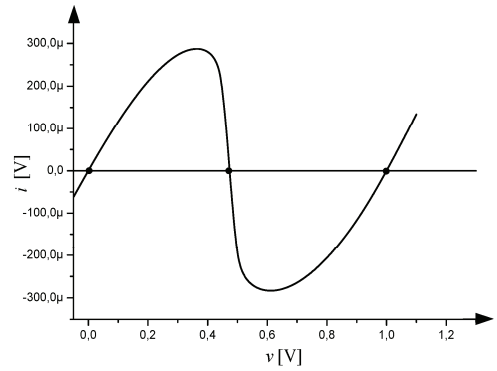

Fig. 4. The test characteristic $i = f(v)$

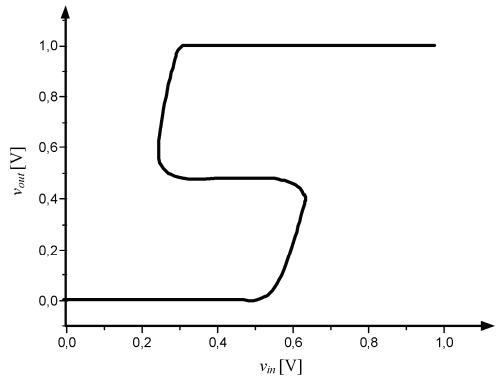

Fig. 5. The input-output characteristic $v_{out} = g(v_{in})$

Conclusion

The proposed algorithm for finding the multiple DC solutions and tracing the multi-valued input-output characteristics enables us to efficiently analyse new generation of integrated circuits, containing MOSFETs characterized by the most advanced compact PSP model.

Acknowledgments: this work was supported by the Ministry of Education and Science under Grant N N515 066435.

REFERENCES

[1] Chua L.O., Lin P.M., Computer-aided analysis of electronic circuits, Algorithms and computational techniques, Prentice-Hall, Inc., 1975

[2] Tadeusiewicz M., „A method for finding bounds on the location of all the solutions of DC piecewise-linear circuits", *Int. J. of Cir. Theor. Appl.*, 18, (1990), 165-174

[3] Tadeusiewicz M., „A method for finding bounds on all the DC solutions of transistor circuits", *IEEE Trans. on Cir. and Syst.*, 39, (1992), 557-564

[4] Tadeusiewicz M., Głowienka K., „A contraction algorithm for finding all the DC solutions of piecewise-linear circuits", *Journal on Cir. Sys. and Comp.*, 4, (1994), 319-336

[5] Pastore S., Premoli A., „Finding all DC solutions of nonlinear resistive circuits by exploring both polyhedral and rectangular circuits", *IEE: Procedings, Circuits, Devices and Systems*, 144, (1997), No. 9, 17–21

[6] Tadeusiewicz M., „DC analysis of circuits with idealized diodes considering reverse bias breakdown phenomenon", *IEEE Trans. on Cir. and Syst.*, 44, (1997), 312-326

[7] Yamamura K., Kameko R., „Finding all solutions of piecewise-linear circuits using simplex method", *IEEE Trans. on Cir. and Syst. – I*, 50, (2003) 160-165

[8] Tadeusiewicz M., Hałgas S., „A method for the analysis of transistor circuits having multiple DC solutions", Int. J. Electron. Commun. (AEU), 60, (2006), No. 8, 582-589

[9] Pastore S., „Fast and efficient search for all DC solutions of PWL circuits by means of oversized polyhedra", *IEEE Trans. on Cir. and Syst. – I*, 58, (2009), 2270-2279

[10] Kolev L.V., Mladenov V.M., „An interval method for finding all operating points of nonlinear resistive circuits", *Int. J. Cir. Theory App.* 18, (1990), 257-267

[11] Ushida A., Yamagami Y., Nishio Y., Kinoichi I., Inoue Y., „An efficient algorithm for finding multiple DC solutions based on the SPICE-oreinted Newton homotopy method", *IEEE Trans. Comput.-Aided Design Integr. Cir. Sig. Process.*, 21, (2002), No. 3, 337-348

[12] Yamamura K., Igarashi N., „An interval algorithm for finding all solutions of non-linear resistive circuits", *Int. J. Cir. Theor. Appl.*, 32, (2004), 47-55

[13] Gajani G.S., Brambilla A., Premoli A., „Numerical determination of possible multiple DC solutions of nonlinear circuits", *IEEE Trans. on Cir. and Syst.-I*, 55, (2008), 1074-1083

[14] Tadeusiewicz M., Hałgas S., „Improved algorithm for computing all the DC operating points of diode-transistor circuits", *The Europ. Conf. on Cir. Theory and Des.,* CD-ROM, (2009), 489-492

[15] Ogorzałek M.J., "Multivalued characteristics in electronic circuits: a unifying approach", *IEEE Trans. Circuits Syst. II*, 47, (2000), 726-735

[16] Tadeusiewicz M., Hałgas S., "Computing multivalued input-output characteristics in the circuits containing bipolar transistors", *IEEE Trans. on Cir. and Syst. –I*, 51, (2004), No. 9, 1859-1867

[17] Tadeusiewicz M., Hałgas S., „Analiza układów nieliniowych o wielu rozwiązaniach DC", *Przegląd Elektrotechniczny*, 85, (2009), No. 11, 149-152

[18] Gildenblat G. et al., "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation", *IEEE Trans. Electron Devices*, 53, (2006), No. 9, 1979-1993

[19] http://pspmodel.asu.edu/

[20] Chua L.O., Kang S.M., „Section-wise piecewise-linear functions: Canonical representation, properties, and applications", *Proc. IEEE* , 65, (1977), 915-929

[21] Kim D., Kih J., Kim W., „A new waveform-reshaping circuit: an alternative approach to Schmitt trigger", *IEEE J. Solid-State Cir.*, 28, (1993), No. 2, 162-164

[22] Hałgas S., Tadeusiewicz M., „Analysis of CMOS circuits having multiple DC operating points", *Proc. 2010 Int. Workshop CPEE 2010*, (2010), 4 pages (CDROM)

***Authors**: dr hab. inż. Stanisław Hałgas and prof. dr hab. inż. Michał Tadeusiewicz, Politechnika Łódzka, Instytut Systemów INżynierii Elektrycznej, ul. Stefanowskiego 18/22, 90-924 Łódź, E-mail: stanislaw.halgas@p.lodz.pl, michal.tadeusiewicz@p.lodz.pl*