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# Simulation of Active Power Filter with prediction control in MATLAB and OrCAD environments with using SLPS interface

***Abstract***. *The newest versions of Cadence's OrCAD packet are equipped with the SLPS interface (SimuLinkPSpice). It allows to carry out simulation of hardware part of tested system in Capture-PSpice simulator and simultaneous simulation of software part of the system in Mathworks' MATLAB-Simulink environment. In the paper use of SLPS interface for modeling Active Power Filter (APF) with prediction control is presented. In OrCAD Capture-PSpice complete 3-phase electric power system including source, nonlinear load and hardware part of APF (especially voltage inverter composed of IGBT transistors) was modelled. In MATLAB-Simulink control system of APF was implemented.*

***Streszczenie.*** *Najnowsze wersje pakietu OrCAD firmy Cadence są wyposażone w interfejs SLPS (SimuLinkPSpice). Pozwala on na przeprowadzenie symulacji części sprzętowej badanego systemu w symulatorze Capture-PSpice tego pakietu oraz równoczesną symulację części programowej w środowisku MATLAB-Simulink firmy Mathworks. W artykule przedstawiono zastosowanie interfejsu SLPS do zamodelowania Energetycznego Filtru Aktywnego (EFA) ze sterowaniem predykcyjnym. W środowisku OrCAD Capture-PSpice zamodelowano kompletny układ 3-fazowy mocy zawierający źródło, nieliniowy odbiornik oraz część sprzętową EFA (w szczególności napięciowy falownik napięcia zbudowany z tranzystorów IGBT). W środowisku MATLAB-Simulink zaimplementowano predykcyjny układ sterowania EFA.*

**Keywords:** active power filter (APF), SLPS interface, OrCAD Capture-PSpice, Matlab-Simulink, prediction control.
**Słowa kluczowe:** energetyczny filtr aktywny (EFA), interfejs SLPS, OrCAD Capture-PSpice, Matlab-Simulink, sterowanie z predykcją.

## SLPS interface

SLPS interface (SimuLinkPSpice) [1, 2, 8, 14] makes possible mutual feedback between two simulators: Capture-PSpice [7] by Cadence™ Design Systems and MATLAB-Simulink [11] by Mathworks™. Thanks to this simulation it is possible to simulate mixed hardware-software projects. Hardware part is simulated in PSpice program, but software part (control algorithm) in MATLAB-Simulink program. The complete simulation of the project is run under control of MATLAB-Simulink, where PSpice simulation model of hardware is visible as special hierarchical circuit. It is possible to specify which input and output signals of this circuit should communicate with software part of the project.

Use of SLPS interface for modeling of Active Power Filter (APF) is presented in the paper. It will be implemented in the near future. The formulated model is designed for carrying out necessary simulation tests preceding final start of APF. The results of simulation will permit verification of correct working of APF and introduction of possible corrections.

## Conception of APF

General aim of APF operation is to improve the quality of energy in 3-phase power system, and, at the same time, chosen parameters determining this quality get better. At present APFs are the subject of numerous research work [5, 6, 9, 12, 15, 16]. Depending on used control algorithm it is possible to obtain together or selectively following effects of improvement of energy quality: elimination of harmonics of phase source input current $i_s$, improvement of power factor, load symmetrization.

In the current paper the task of APF is to filter source current $i_s$ harmonics, so that current $i_s$ will be sinusoidal regardless of how big the deformation of the load current $i_L$ is. The control algorithm is based on instantaneous power theory, in particular one of its generalizations, which takes advantage of d-q rotational coordinates transformation [3]. APF with parallel topology was chosen (Fig. 1). In this variant APF is compensation current source $i_k$, which is put parallel to the power grid system at a point between source and load. Current $i_k$ must be produced in real time following-up changes in load current $i_L$, so that source current $i_s$ ($i_s = i_k + i_L$) is sinusoidal. APF is composed of the power electronics voltage inverter with PWM modulation and inductor $L_k$ used to shape current $i_k$ in follow-up mode.

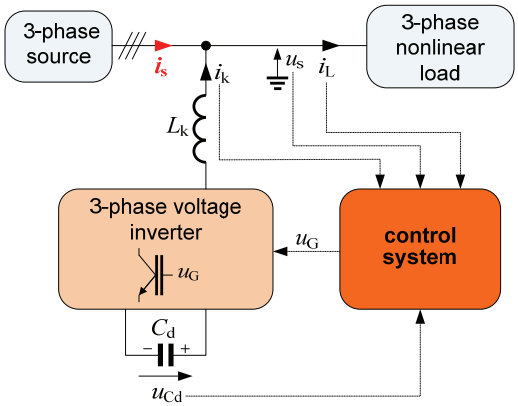


Fig. 1. Block diagram of 3-phase electric power system with nonlinear load and parallel APF with open control system

The voltage inverter is full 3-phase IGBT transistor bridge. Gates of transistors are controlled by the control system, which operates with open configuration – compensated quantity (result of filtering) $i_s$ is not transmitted

back into input of the control system (no feedback). Control system requires measurements: phase load current $i_L$, phase compensation current $i_k$, phase network voltage $u_s$ and voltage $u_{Cd}$ on supply capacitor $C_d$.

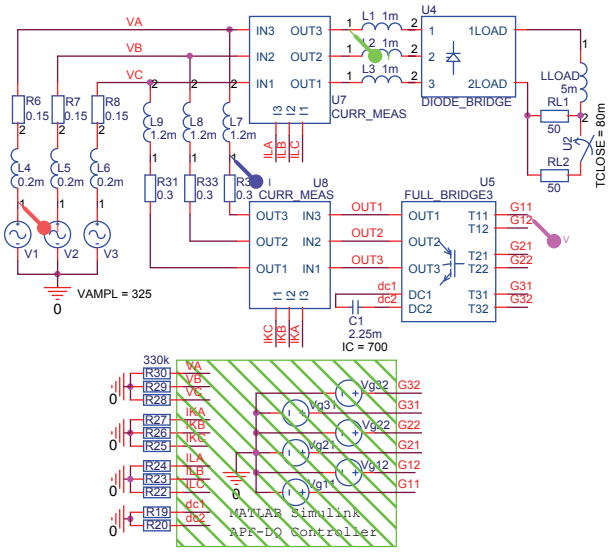


Fig. 2. The Capture-PSpice hardware simulation circuit of 3-phase power system with active power filter

**Simulation model of hardware circuit**

The hardware part of complete 3-phase electric power system was modeled in Capture-PSpice environment (Fig. 2). The model includes supply source, nonlinear load and APF. In this model impedance of power supply line was taken into consideration. Assumptions of the model are as follows:

- 3-phase 325 V amplitude voltage generator (sources V1, V2, V3),
- nonlinear load: 6-pulse diode bridge (U4) loaded by resistor RL1 = 50 Ω (total active absorbed power $P_c$ about 6 kW), after time $t_o$ = 80 ms resistor RL2 = 50 Ω is added, connected in parallel (increase of $P_c$ to about 12 kW),
- impedance of power supply line between source and point of placing EFA: resistance 0,15 Ω in series with inductance 0,2 mH (L4-R6, L5-R7, L6-R8),
- inductance of power supply line between point of placing EFA and load (L1, L2, L3): 1 mH,
- Active Power Filter (APF) composed of full IGBT transistor bridge (U5) and compensation current shaping inductors $L_k$ (L7, L8, L9),
- IGBT bridge supplied from capacitor C1 with dc link voltage Ucd=700V,
- inductance of shaping inductors $L_k$: 1,2 mH,
- shaping inductors resistance $R_k$ is assumed to be non-zero (R31, R32, R33): 0,3 Ω,
- bridge (U5) is composed of IGBT transistors IRG4PH50U,
- frequency of PWM: $f_{PWM}$ = 20 kHz.

This model takes into consideration measurement circuits of phase currents: load current (U7) and compensation current (U8). These circuits convert current signals to voltage signals with conversion coefficient 1 V/A: ILA, ILB, ILC – measurement results of load currents, IKA, IKB, IKC – measurement results of compensation currents. Fig. 2 shows control system area implemented in MATLAB-Simulink environment, it is marked with dashed lines. Output signals of the control system are transmitted back into hardware part model through VSRC type sources (Vg11, Vg12, Vg21, Vg22, Vg31, Vg32). These signals control gates of transistors bridge U5 (nodes: G11, G12, G21, G22, G31, G32). The control system receives following input signals from the hardware part model:

- VA, VB, VC – phase network voltages at point of APF placing,
- IKA, IKB, IKC – phase compensation currents produced by APF,
- ILA, ILB, ILC – phase load currents,
- dc1, dc2 – supply capacitor C1 voltage.

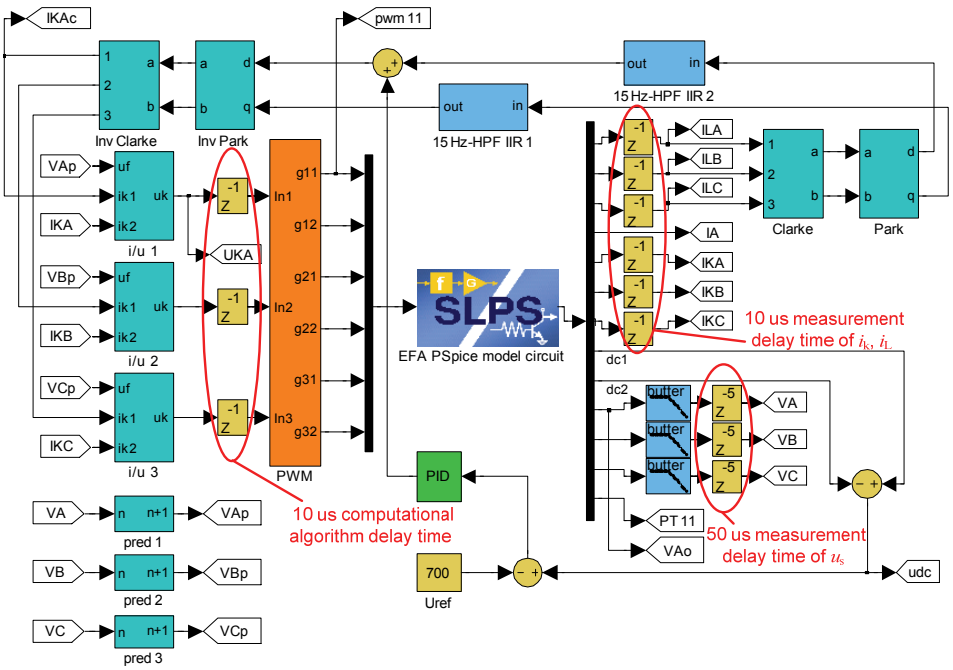


Fig. 3. The APF control system implemented in MATLAB-Simulink environment

**Simulation model of control system**

Block diagram of the control system has been created in MATLAB-Simulink environment, it is composed of ready-made toolboxes, which are available in this environment (Fig. 3). The circuit of hardware part of system model (Fig. 2) (created in Capture-PSpice) is visible as special hierarchical circuit block – it is toolbox named SLPS. In the SLPS block it is possible to define which input and output signals of the hardware model must be visible in the control system model. The control system realizes algorithm based on instantaneous power theory, in particular one of its generalizations, which takes advantage of d-q rotational coordinates transformation [3]. The heart of the system is PWM modulator ('PWM' block), operating at frequency $f_{PWM}$= 20kHz. It directly controls gates of inverter transistors.

Standard of compensation currents $i_k$ ('Inv Clarke' block – signals: 1, 2, 3) is calculated on the basis of phase load currents $i_L$ (ILA, ILB, ILC) using simple and inverse Park and Clark transform (blocks: 'Clarke', 'Park', 'Inv Park', 'Inv Clarke',' IIR1' and 'IIR2' – indispensable IIR digital lowpass filters with 15 Hz cut-off frequency). In case of subsequent phases the created standard $i_k$ (signal ik1) is converted to input voltage of PWM modulator (signal uk) on the basis of actual value of phase voltage $u_s$ (signal uf), according to principle showed in Fig. 4. Implementation of the 'i/u' block is presented in Fig. 5. Nominal values $R_k$, $L_k$: $R_k$ = 0.3 Ω, $L_k$ = 1.2 mH are set in this block.

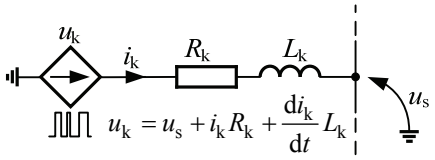


Fig. 4. Conversion idea of compensation current standard $i_k$ to inverter input voltage $u_k$

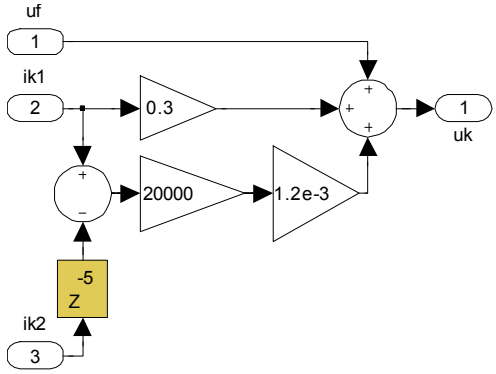


Fig. 5. Implementation of the 'u/i' block

Derivative of current $i_k$ is calculated numerically as increment of this current over time equal to one cycle of PWM processing:

$$(1) \qquad \frac{\Delta i_k}{\Delta t} = \frac{i_{k1} - i_{k2}}{T_{PWM}} = (i_{k1} - i_{k2}) f_{PWM},$$

where: $i_{k1}$– actual calculated value of standard $i_k$, $i_{k2}$ – value of current $i_k$ measured in previous PWM cycle ('$z^{-5}$' block carries out 50 μs processing delay with sampling every 10 μs), $T_{PWM} = 1/f_{PWM}$ = 50 μs – PWM processing period.

Network voltage $u_s$ is in reality measured with delay amounting to about 50 μs (this is taken into consideration in '$z^{-5}$' blocks), moreover inverter produces compensation current with $T_{PWM}$ = 50 μs delay. When all these points are considered, calculation of standard $i_k$ is incorrect, and this in turn causes deterioration of harmonics filtering of current $i_s$. The error is visible especially at time instants when $i_L$ course changes violently, and this takes place in modeled 3-phase system. The error of standard $i_k$ can be decreased by calculating phase lead course of voltage $u_s$ with shift time taking into consideration mentioned delays. Linear prediction is used to phase-lead shift of course $u_s$ [10, 13]. Its principle is illustrated in Fig. 6 by example of voltage course $u(t)$ shifted with prediction time $t_p$. Future voltage value $u'_{k+1}$ is calculated on the basis of present value $u_k$ and preceding value $u_{k-1}$, according to formula:

$$(2) \qquad u'_{k+1} = 2u_{k-1} - u_k .$$

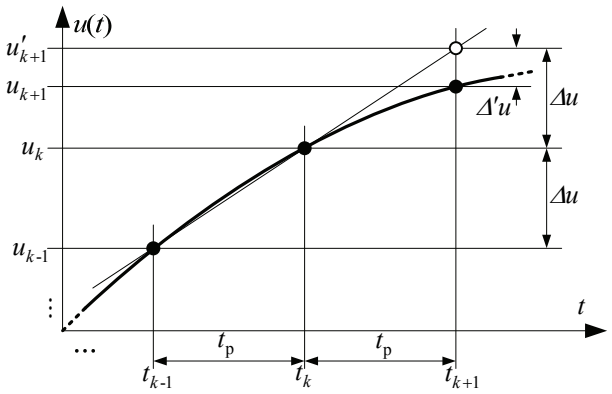


Fig. 6. Idea of linear prediction of voltage $u(t)$

Prediction of value $u'_{k+1}$ is burdened with error $\Delta' u$ : the shorter the prediction time $t_p$, the smaller the error. Switching operation of APF produces lots of noise in voltage course $u_s$. In order that the noise does not penetrate to the standard $i_k$, voltage $u_s$ is initially smoothed in lowpass Butterworth filter ('Butter' block). Prediction block of voltage $u_s$ (Fig.7) takes into consideration additional delay produced by smoothing filter (prediction time amounts to $\Delta t$ = 180 μs with sampling every 10 μs). Fig. 8 shows simulation voltage $u_s$ courses: directly after measurement, after smoothing filtering and after prediction use.

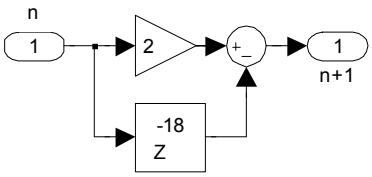


Fig. 7. Implementation of the 'pred' block

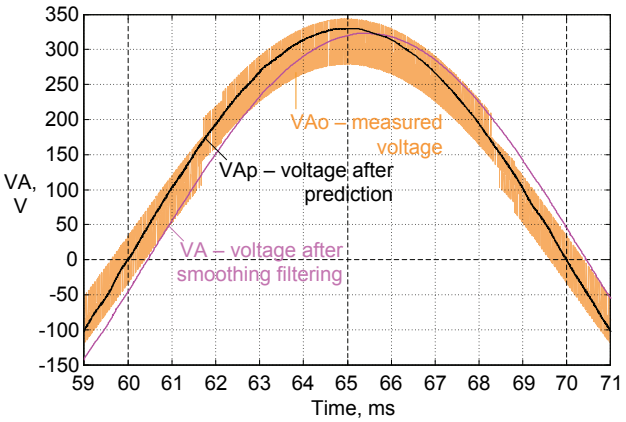


Fig. 8. Simulation courses of voltage $u_s$ for phase 1 (phase a): VAo - directly after measure, VA – after smoothing filtering, VAp – after prediction

Supply capacitor voltage (signal udc) is monitored and in feedback path (PID controller is inserted in feedback loop) it is kept at 700 V level. Model of the control system takes into consideration measurement delay of phase currents: load current, compensation current, measurement delay of phase voltage, it also takes into consideration computational time-lag (delay time 10 μs, 'z-1' blocks).

**MATLAB-Simulink simulation results**

Chosen simulation results obtained in MATLAB-Simulink environment are shown in Fig.9. Current IKA (L1 phase) generated in APF compensates deformation of load current ILA (L1 phase), thanks to this input source current IA (L1 phase) is approximately sinusoidal. THD coefficient of current IA calculated accurate up to 40th harmonic confirms that. It amounts to about 3.5% for RL = 50 Ω and only about 2.0% for RL = 25 Ω, and this is substantial improvement with relation to THD coefficient value of load current – about 21%. Compensation current standard IKA is concurrent with APF output current IKA, this additionally confirms correct operation of whole 3-phase system. Stabilization of supply capacitor voltage ucd operates correctly. Voltage ucd falls down by about 10 V only during step change in load, apart from that it is kept at 700 V level with very small pulsation present (about 2 V).

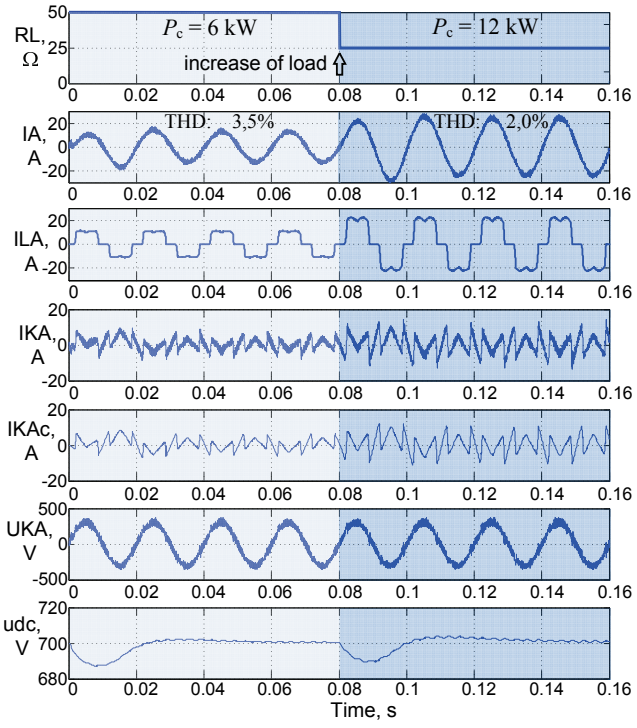


Fig. 9. Chosen simulation results from MATLAB-Simulink environment: RL – load resistance, IA – source current (L1 phase), ILA – load current (L1 phase), IKA – APF output compensation current (L1 phase), IKAc – standard of compensation current (L1 phase), UKA – input voltage of PWM modulator (L1 phase), udc – supply capacitor voltage

**Capture-PSpice simulation results**

Exemplary simulation results obtained in Capture-PSpice environment are shown in Fig. 10.

Fig.10 presents following current waveforms for L1 phase over one period of power grid voltage (20 ms): load current, APF current and final effect of filtering - sinusoidal source current course. In these courses high frequency components (20 kHz) are visible, their presence results from APF operating in switching-mode.

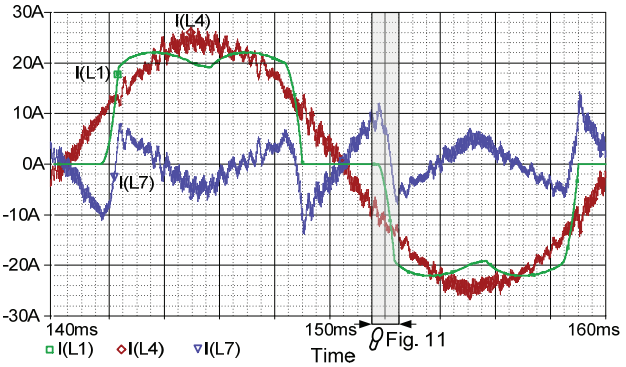


Fig. 10. Chosen simulation results for L1 phase from Capture-PSpice environment: I(L1) – load current, I(L7) – output current of APF, I(L4) – source current

Fig. 11 shows, for a narrow time interval (1 ms) and L1 phase, how PWM signal controlling inverter influences APF current course I(L7). Linear change of current I(L7) (alternately positive and negative) responds to every step change of PWM signal (alternately down and up), that results from these courses.


Fig. 11. Chosen simulation results for L1 phase from Capture-PSpice environment: V(G11) – PWM voltage inverter control signal and output EFA current I(L7) corresponding to this signal

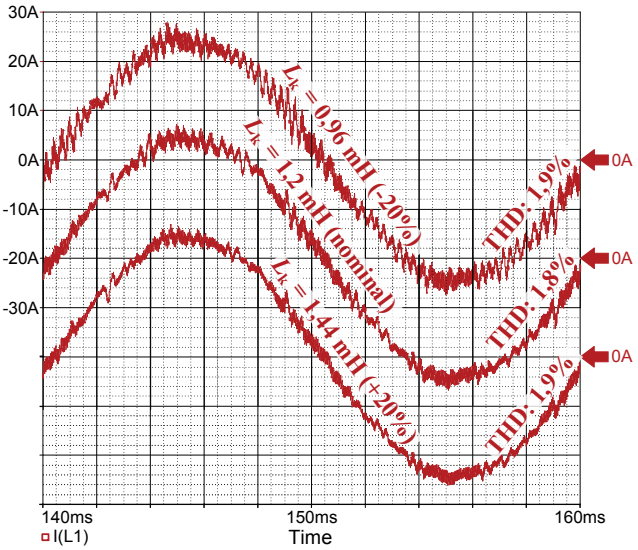


Fig. 12. Source current for 3 values of $L_k$: nominal ($L_k$=1.2 mH), nominal -20% ($L_k$ = 0.96 mH), nominal +20% ($L_k$ = 1.44 mH)

'u/i' block of the control system is set for nominal values $R_k$, $L_k$, and these values in reality can differ from nominal ones, and especially $L_k$. That is why it was tested how input source current is shaped after using APF filtering for three

values of $L_k$: nominal (1.2 mH), decreased by 20% (0.96 mH), increased by 20% (1.44 mH). The result is presented in Fig. 12. The courses insignificantly differ, and THD measurement confirms this fact. Therefore it is possible to affirm, that system will work correctly, even if inductance $L_k$ differs from nominal value by ±20%.

**Summary**

Complex circuits controlled by the control system implemented in MATLAB-Simulink environment in block diagram form may be modeled with SLPS interface. What is important is that control system modeled in such a way can carry out discrete-time algorithm, which is not possible in case of the modeling in Capture-PSpice environment [4] (using ABM library). Modeling of circuits in Capture-PSpice environment is more reliable than in MATLAB-Simulink environment. To recapitulate: SLPS interface creates new possibilities of hardware-software system simulation. It ensures better results than use of single simulation environment only.

Fig. 13. Intelligent power modules MITSUBISHI PM75CL1A120: 3-phase, 75A, 1200V, current-sense and temperature sense IGBT type inverter

In the paper SLPS interface is used to model complete 3-phase power system including: generator, nonlinear load and APF (IGBT inverter based) along with the control system, which carries out discrete-time control algorithm based on instantaneous power theory. Created whole system model will be helpful in construction of the APF prototype. Control system model takes into consideration measurement and computational delays which occur in reality. Obtained simulation results are satisfactory. However simulations will be continued, because in present version the system is simulated by using models of quite high-speed IGBT transistors (transistors IRG4PH50U can operate with switching frequency up to 40 kHz), whereas the planned prototype of APF will be based on integrated transistors bridge MITSUBISHI PM75CL1A120 (Fig. 13), which is slower (it will operate with switching frequency of maximum frequency 16 kHz). Moreover the aforementioned bridge will be equipped with dedicated hardware controller. The subsequent simulations will focus on modeling the target bridge along with its hardware controller, so that analysis of operating system will be possible its implementation in real life.

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*This research work is financed from financial resources on science in years 2008-2011 as research project N N510 344634*



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