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Phase locked loop and synchronization methods for grid-interfaced converters: a review

Abstract. *Phase locked loop and synchronization techniques are one of the most important issues for operating grid-interfaced converters in practical applications, which involve Distributed Power Generation Systems, Flexible AC Transmission Systems (FACTS), and High Voltage Direct Current (HVDC) Transmission, and so on. This paper presents a comprehensive review of the recently developed phase locked loop and synchronization methods, then a comparison and selection guide are provided. Finally, a list of more than 40 technical papers is also appended for a quick reference.*

Streszczenie. *Techniki PLL i synchronizacji są ważnymi elementami przetworników w systemach sieciowych, takich jak: rozproszonych systemach mocy, FACTs czy HVDC. Artykuł przedstawia przegląd tego typu metod a następnie porównanie tych metod. Na końcu ponad 40 podstawowych artykułów z tej tematyki jest przedstawionych.(**Metody synchronizacji i PLL w przetwornikach sieciowych – przegląd**).*

Keywords: Grid-interfaced converters, phase locked loop, synchronization
Słowa kluczowe: uchłady PLL, synchronizacja.

Introduction

The basic phase locked loop (PLL) concept was originally published by Appleton in 1923 and Bellescize in 1932, which was mainly used for synchronous reception of radio signals [1-2]. After that, PLL techniques were widely used in various industrial fields such as communication systems [3-6], motor control systems [7-8], induction heating power supplies [9] and contactless power supplies [10].

Recently, PLL techniques have been used for synchronization between grid-interfaced converters and the utility network. An ideal PLL can provide the fast and accurate synchronization information with a high degree of immunity and insensitivity to disturbances, harmonics, unbalances, sags/swells, notches and other types of distortions in the input signal. This paper aims at presenting a comprehensive survey on various PLL synchronization techniques to facilitate the proper selection for specific applications.

PLL synchronization techniques

The most widely accepted synchronization solution to a time-varying signal can be described by the basic structure shown in block diagram form in Fig. 1, where the difference between phase angle of the input and that of the output signal is measured by the phase detection (PD) and passed through the loop filter (LF). The LF output signal drives the voltage-controlled oscillator (VCO) to generate the output signal, which could follow the input signal.

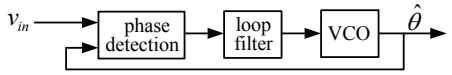

Fig.1 Closed-loop synchronization structure

1 SF-PLL

Synchronous Frame PLL (SF-PLL) is widely used in three-phase systems. The block diagram of SF-PLL is illustrated in Fig.2, where the instantaneous phase angle θ is detected by synchronizing the PLL rotating reference frame to the utility voltage vector. The PI controller sets the direct or quadrature axis reference voltage v_d or v_q to zero, which results in the reference being locked to the utility voltage vector phase angle. In addition, the voltage frequency f and amplitude v_m can be obtained as the by-products. Under ideal utility conditions without any harmonic distortions or unbalance, SF-PLL with a high bandwidth can yield a fast and precise detection of the phase and amplitude of the utility voltage vector. In case the utility voltage is distorted with high-order harmonics, the SF-PLL can still operate if its bandwidth is reduced at the cost of the PLL response speed reduction in order to reject and cancel out the effect of these harmonics on the output. However, the PLL bandwidth reduction is not an acceptable solution in the presence of the unbalanced utility voltage [11-12]. Note that, the amplitude, phase and frequency values provided by SRF-PLL are not individual-phase but average information, and SRF-PLL may not be applied to single-phase systems in a straightforward manner. However, it provides a useful structure for single-phase PLLs as long as the 90-degree-shifted orthogonal component of the single-phase input signal is created [13].

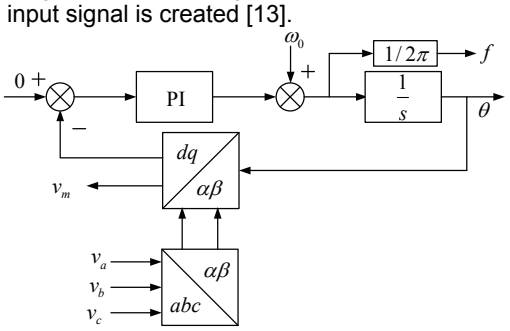

Fig.2 Block diagram of SF-PLL

2 PQ-PLL

Rolim et al. [14] point out that PLL may fail in tracking the system voltage during startup under some adverse conditions, and oscillations caused by the presence of subharmonics can pull the stable point of operation synchronized to the subharmonic frequency. In order to settle these problems, a robust digital synchronizing PLL based on the instantaneous real and imaginary power theory (PQ-PLL) is presented to maintain synchronization in presence of subharmonics, harmonics, and negative-sequence unbalances. The block diagram of PQ-PLL is shown in Fig.3.

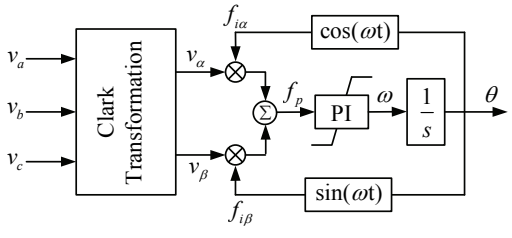

Fig.3 Block diagram of PQ-PLL

It has the similar structure to the conventional SF-PLL, but it can be easily understood from the viewpoint of the instantaneous power theory. Besides, the fundamental positive-sequence components can be obtained as a by-product.

3 DSF-PLL

Double Synchronous Frame PLL (DSF-PLL) [15-16] is based on transforming both the positive and negative sequence components of the utility voltage into the double synchronous frame, which can completely eliminate the detection errors of the conventional SF-PLL. The block diagram of DSF-PLL is shown in Fig.4.

Its unique decoupling network can cancel out the double frequency oscillations at 2ω in $v_{q^+}^*$, therefore, there is no need to reduce the PLL bandwidth for the accurate positive-sequence component estimation compared with the conventional SF-PLL. It is very suitable to the control of grid-interfaced converters operating in the severe frequency derivation and unbalanced conditions.

(1)
$$\begin{bmatrix} v_{d^+} \\ v_{q^+} \end{bmatrix} = \begin{bmatrix} v_{d^+}^* \\ v_{q^+}^* \end{bmatrix} + \begin{bmatrix} \tilde{v}_{d^+} \\ \tilde{v}_{q^+} \end{bmatrix} \qquad \begin{bmatrix} \tilde{v}_{d^+} \\ \tilde{v}_{q^+} \end{bmatrix} = \begin{bmatrix} \cos(2\theta) & \sin(2\theta) \\ -\sin(2\theta) & \cos(2\theta) \end{bmatrix} \begin{bmatrix} \bar{v}_{d^-} \\ \bar{v}_{q^-} \end{bmatrix}$$

$$\begin{bmatrix} v_{d^+}^* \\ v_{q^+}^* \end{bmatrix} = \begin{bmatrix} v_{d^+} \\ v_{q^+} \end{bmatrix} - \begin{bmatrix} \cos(2\theta) & \sin(2\theta) \\ -\sin(2\theta) & \cos(2\theta) \end{bmatrix} \begin{bmatrix} \bar{v}_{d^-} \\ \bar{v}_{q^-} \end{bmatrix}$$

(2)
$$\begin{bmatrix} v_{d^-} \\ v_{q^-} \end{bmatrix} = \begin{bmatrix} v_{d^-}^* \\ v_{q^-}^* \end{bmatrix} + \begin{bmatrix} \tilde{v}_{d^-} \\ \tilde{v}_{q^-} \end{bmatrix}$$

$$\begin{bmatrix} \tilde{v}_{d^-} \\ \tilde{v}_{q^-} \end{bmatrix} = \begin{bmatrix} \cos(-2\theta) & \sin(-2\theta) \\ -\sin(-2\theta) & \cos(-2\theta) \end{bmatrix} \begin{bmatrix} \bar{v}_{d^+} \\ \bar{v}_{q^+} \end{bmatrix}$$

$$\begin{bmatrix} v_{d^-}^* \\ v_{q^-}^* \end{bmatrix} = \begin{bmatrix} v_{d^-} \\ v_{q^-} \end{bmatrix} - \begin{bmatrix} \cos(-2\theta) & \sin(-2\theta) \\ -\sin(-2\theta) & \cos(-2\theta) \end{bmatrix} \begin{bmatrix} \bar{v}_{d^+} \\ \bar{v}_{q^+} \end{bmatrix}$$

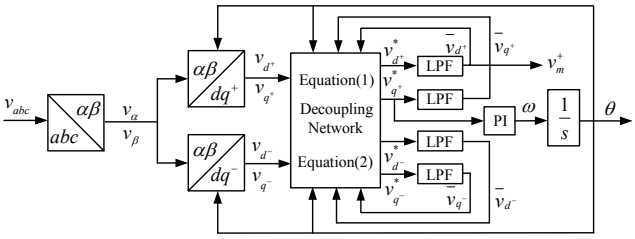

Fig.4 Block diagram of DSF-PLL

4 SSI-PLL

Sinusoidal Signal Integrator PLL (SSI-PLL) [17-18] tracks the utility voltage by extracting the fundamental positive sequence to the SF-PLL. Therefore, it operates well under voltage distortions and imbalances. The block diagram of SSI -PLL is shown in Fig.5, where the constant K controls the bandwidth and the response speed of the SSI-PLL. On the other hand, there is another similar structure with a single SSI shown in Fig.6, where the positive-sequence component v_α^+ is extracted by using a single SSI acting as a filter for the measured utility voltage, and v_β^+ is calculated from v_α^+ by delaying 90 degrees. Constant K controls the filtering response and the PLL bandwidth. The sign is chosen by a sequence detector. If the voltage sequence at the PCC is known in advance, the sequence detector can be eliminated. The main advantages of SSI-PLL are immunity to the voltage distortion and unbalance. In addition, it can be extended into the single-phase system applications with a few modifications.

5 DSOGI-PLL

Double second order generalized integrator PLL (DSOGI-PLL) [19-21] is similar to SSI-PLL, which extracts the fundamental positive sequence to the SF-PLL. But it utilizes

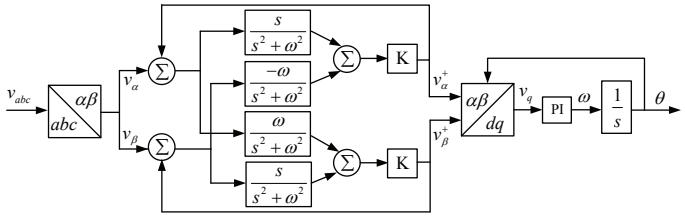

Fig.5 Block diagram of PLL with multiple SSIs

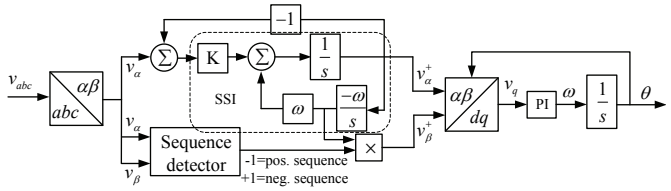

Fig.6 Block diagram of PLL with single SSI

a double second order generalized integrator to implement the quadrature-signals generator. The three-phase voltage vector can be expressed as $v_{abc} = \begin{bmatrix} v_a & v_b & v_c \end{bmatrix}^T$, and its positive sequence component can be obtained as follows:

(3)
$$v_{\text{abc}}^+ = \begin{bmatrix} v_{\text{a}}^+ & v_{\text{b}}^+ & v_{\text{c}}^+ \end{bmatrix}^T = [T] v_{\text{abc}}$$

$$[T] = \frac{1}{3} \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \qquad a = e^{-j\frac{2\pi}{3}}$$

And then the positive-sequence component of the voltage vectors can be obtained as follows:

(4)
$$v_{\alpha\beta}^+ = C_{32} v_{\text{abc}}^+ = C_{32}[T] v_{\text{abc}} = C_{32}[T] C_{23} v_{\alpha\beta} = \frac{1}{2} \begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} v_{\alpha\beta}$$

$$C_{32} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \qquad C_{23} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}^T$$

In the same way, the negative-sequence component of the voltage vectors can be also obtained as follows:

(5)
$$v_{\alpha\beta}^- = \frac{1}{2} \begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} v_{\alpha\beta} \qquad q = e^{-j\pi/2}$$

Therefore, the accurate sequence component extraction here requires 90-degree phase shift for v_α and v_β. There are two solutions for this purpose. They are the transport delay buffer method and the all pass filter method. However, such methods are not frequency-adaptive, which could give rise to errors in the positive sequence estimation. Moreover, they can't block harmonics from the input signals. In order to solve these problems, a smart combination of a low pass filter (LPF) and a band-pass filter (BPF) is utilized, where the BPF (6) only provides harmonic-filtering functions but the LPF (7) offers both the harmonic filtering and 90-degree phase shift. Besides, the filter parameter ω is updated from the PLL for the frequency-adaptive purpose. The block diagram is shown in Fig.7.

(6)
$$BPF(s) = \frac{v'}{v} = \frac{k\omega s}{s^2 + k\omega s + \omega^2}$$

$$LPF(s)=\frac{qv'}{v}=\frac{k\omega^2}{s^2+k\omega s+\omega^2} \quad (7)$$

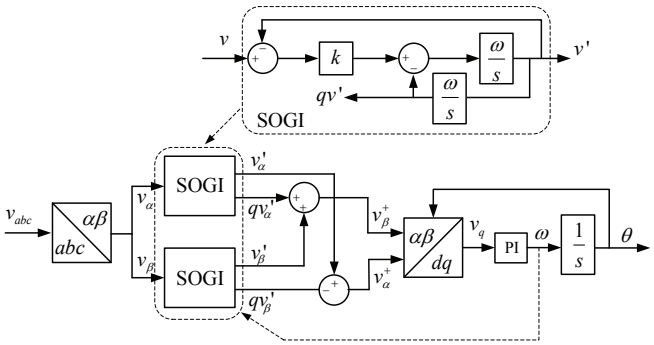

Fig.7 Block diagram of DSOGI-PLL

Having the same principle as SSI-PLL, DSOGI-PLL extracts the fundamental positive sequence v_α^+ and v_β^+ to the conventional SF-PLL. Therefore, it can provide the accurate positive sequence information for grid synchronization even under grid faulty conditions. In addition, it can be also extended into the single-phase system applications as SSI-PLL because 90-degree phase shift information can be easily obtained.

6 EPLL

Enhanced phase-locked loop (EPLL) [22-24] is a frequency-adaptive nonlinear synchronization approach. The block diagram of EPLL is shown in Fig.8 and Fig.9.

Its major improvement over the conventional PLL lies in the PD mechanism which allows more flexibility and provides more information such as amplitude and phase angle. There are three independent internal parameters K , K_pK_v and K_iK_v . Parameter *K* dominantly controls the speed of the amplitude convergence. K_pK_v and K_iK_v control the rates of phase and frequency convergence.

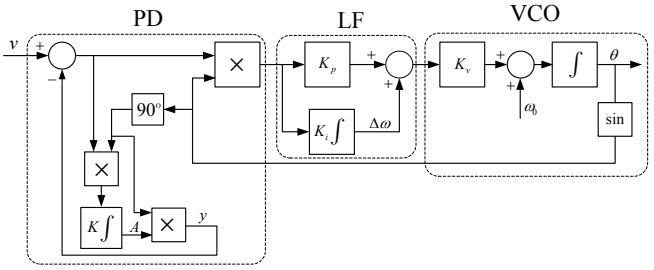

Fig.8 Block diagram of single-phase EPLL

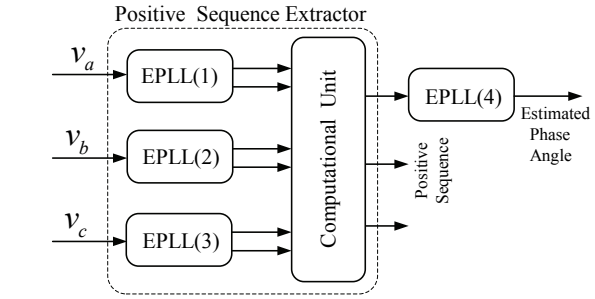

Fig.9 Block diagram of three-phase EPLL

EPLL can provide higher degree of immunity and insensitivity to noise, harmonics and unbalance of the input signal. It is an effective method for synchronization of the grid-interfaced converters in polluted and variable-frequency environments. In addition, EPLL can provide the 90 degrees shift of the input signal. Therefore, it is an attractive solution in some single phase system applications.

7 3MPLL

Three-phase magnitude phase locked loop (3MPLL) adaptively tracks and estimates the magnitude, phase angle, and frequency of the input signal [25]. The block diagram is shown in Fig.10, which can be mathematically described with the differential equations (8).

$$\begin{cases} \dot{V}=\mu_v[e_a\sin\phi+e_b\sin(\phi-\frac{2\pi}{3})+e_c\sin(\phi+\frac{2\pi}{3})] \\ \dot{\omega}=\mu_\omega[e_a\cos\phi+e_b\cos(\phi-\frac{2\pi}{3})+e_c\cos(\phi+\frac{2\pi}{3})] \\ \dot{\phi}=\omega+\mu_\delta\dot{\omega} \end{cases} \quad (8)$$

The performance of 3MPLL is controlled by three controlling parameters μ_v , μ_ω and μ_δ , It is an extension of the already presented single-phase PLL [26-27]. Particularly, it can be used as a three-phase nonlinear anti-aliasing filter with no phase-shift and no amplitude bias. Three unique features of such a filter are frequency adaptation, distortion/unbalance mitigation, structural simplicity and robustness.

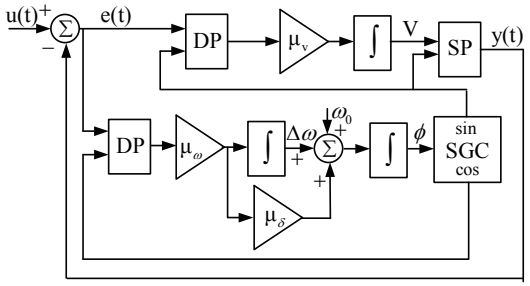

Fig.10 Block diagram of 3MPLL

8 QPLL

The operation principle of this phase-locked approach is based on estimating in-phase and quadrature-phase amplitudes of the fundamental component of the input signal and thus is called quadrature PLL (QPLL) [28]. The block diagram is shown in Fig.11, where its output *y*(*t*) can be formulated as a sum of the in-phase and quadrature-phase components.

$$y(t)=K_s(t)\sin\phi(t)+K_c(t)\cos\phi(t) \quad (9)$$

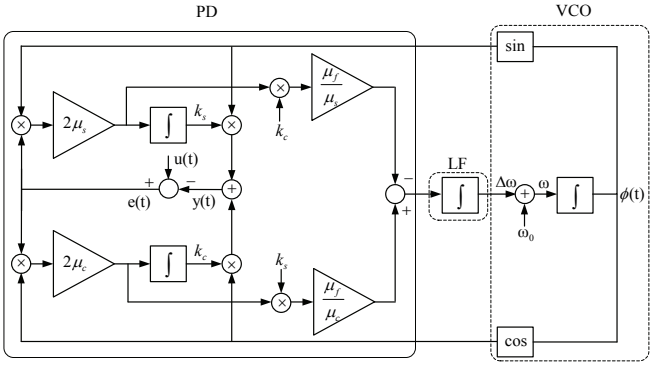

Fig.11 Block diagram of QPLL

Parameters μ_s , μ_c and μ_f control the behavior of QPLL, which correspond to the in-phase and quadrature-phase amplitudes and frequency respectively.

QPLL can provide a precise estimation of the in-phase amplitude K_s, quadrature amplitude K_c and phase $\phi(t)$ in

an adaptive way. It is applicable to both the distributed generation and communication system applications.

9 RPLL

Shinnaka has recently proposed a robust single-phase PLL (RPLL) structure [29-30] shown in Fig. 12. It consists of a two-phase signal generator, a vector rotator, a low-pass filter, a phase synchronizer and a multirate sample-holder.

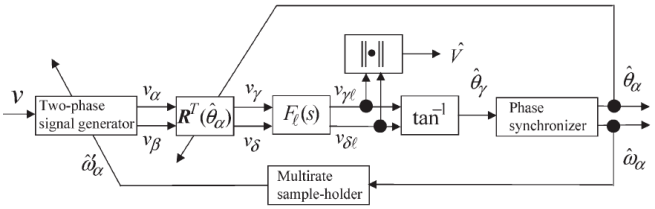

Fig.12 Block diagram of RPLL

Different from other single-phase PLLs, the phase synchronizer is based on the "generalized integral-type PLL method" [31]. And the unique multirate sample-holder keeps the output to be constant for a specified holding period even for varying input so as to avoid the instability phenomena due to instant reuse of the frequency estimate. Besides, an important observation pointed out by Shinnaka is that the differential-type two-phase signal generator is better than the integral-type one in transients. This robust single-phase PLL can instantly estimates the phase, frequency, and amplitude information of single-phase signals with frequency variation, phase jump, amplitude sag/swell, harmonics distortion, and/or contaminated noise.

10 PPLL

Predictive phase locked loop (PPLL) is a wide-range synchronization method [32]. The block diagram of PPLL is shown in Fig.13. It is comprised of a predictor, oscillator, phase-shifter, and data acquisition blocks. Its phase locking mechanism is similar to the conventional PLL in the sense that PPLL locks to the phase of input signals, but it employs the analytical expressions for computing the frequency, amplitude and phase difference in a predicted manner. The predictor is the core of PPLL. It acquires three $120°$ equidistant samples from the input signal: s_0 , s_{120} , s_{240} , which are used to characterize one period of a sinusoidal waveform.

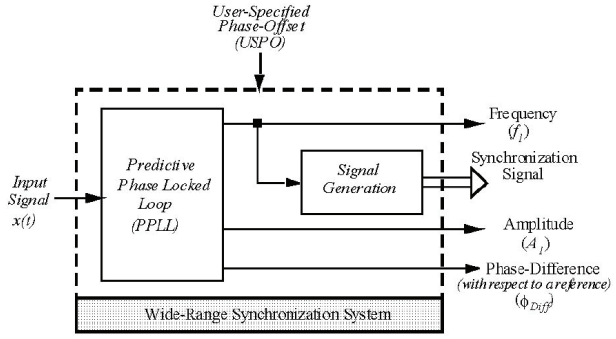

Fig.13 Block diagram of PRPLL

Its unique feature lies in the wide-range synchronization capability. Besides, the synchronization information can be extracted within two cycles of the input signal period under the worst cases such as perturbations in frequency, amplitude and phase angle.

11 ALC-PLL

B. Han [33] proposed a novel PLL that is composed of adaptive linear combiner (ALC) and the proportional integral control. The block diagram is shown in Fig.14. The associated formulae are as follows:

$$(10)\quad \begin{cases} V_M \sin(\omega t+\phi) = V_{M\sin}\sin(\omega t+\theta^*) + V_{M\cos}\cos(\omega t+\theta^*) \\ \hat{Y} = [W_1 \;\; W_2]\begin{bmatrix} X_1 \\ X_2 \end{bmatrix} = [V_{M\cos} \;\; V_{M\sin}]\begin{bmatrix} \sin(\omega t) \\ \cos(\omega t) \end{bmatrix} \end{cases}$$

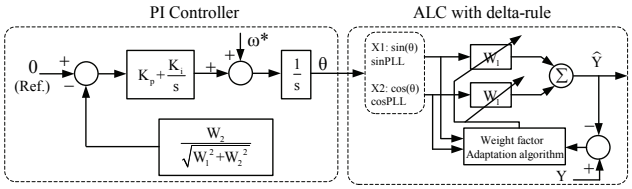

Fig.14 Block diagram of ALC-PLL

ALC-PLL forces the value of $V_{M\cos}$ to zero, and thus the phase angle of X_1 will track the fundamental component of the input signal. It can provide the accurate performance in phase locking under the voltage disturbances, such as sag, harmonics, unbalance, and phase-angle jump.

12 MR-PLL

The multirate PLL (MR-PLL) is a variable sampling-rate system. Compared with the single-rate PLL, it operates at two different sample rates. One sample rate is much higher than the input-signal (carrier) frequency and the other sample rate is equal to the carrier frequency. MR-PLL can provide accurate phase synchronization to severely disturbed signals, and it is an all-digital approach [34]. The disturbance rejection is mainly determined by the frequency response of a high-order band-pass anti-aliasing filter, which provides more disturbance rejection compared to other approaches [35]. The anti-aliasing filter automatically adapts to the input-signal-frequency variations through the system's variable sample-rate operation, which is achieved by modifying the processor timer and applying the over-sampling technique to the input signal.

13 APLL

The adaptive PLL (APLL) regulates the system gain in an adaptive manner [36]. It consists of three control units that individually control frequency, phase angle and voltage magnitude. The voltage controller output is used to compensate the reduced gain caused by voltage sag. The output phase angle and its derivative, the frequency signal, are controlled to enable elimination of frequency and phase error without compromising transient responses. The main advantages of the adaptive PLL is that settling time and overshooting are significantly lower in case of reduced ac voltage magnitude.

14 Other synchronization methods

The simplest synchronization solution is the zero-crossing-detection (ZCD) method shown in Fig. 15, where the zero-crossing point is detected every one period and the sin-table pointer is reset from scratch. It can be only used where the input is a stable and sinusoidal signal due to its sensitivity to transient and noise [37].

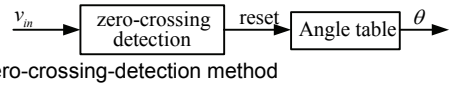

Fig.15 Zero-crossing-detection method

Space Vector (SV) method is another synchronization solution. The basic idea of SV method is to detect the angular frequency of the space vector $v = v_\alpha + jv_\beta$ [38]. The

block diagram is shown in Fig.16. The instantaneous angular frequency can be obtained as follows:

$$\omega_v = \frac{d}{dt}(\text{atan}\frac{v_\beta}{v_\alpha}) = \frac{v_\alpha \frac{dv_\beta}{dt} - v_\beta \frac{dv_\alpha}{dt}}{v_\alpha^2 + v_\beta^2} \quad (11)$$

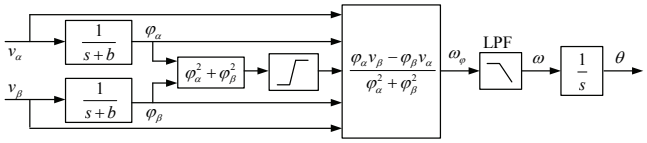

Fig.16 Space vector method

In order to avoid the numerical derivations in (11), another approach should be envisaged. The following space vector $\varphi = \varphi_\alpha + j\varphi_\beta$ is considered by applying to the space vector the transfer function

$$\varphi(s) = \frac{1}{s+b} v(s) \quad (12)$$

where *b* is a damping coefficient that ensures the asymptotic stability of (12). Note that with *b*=0, (12) would be sensitive to the initial conditions and would accumulate errors.

In steady state, the vector v has the same average frequency as φ, while the instantaneous frequencies are different. The expression (11) of the angular frequency can be applied to the vector as

$$\omega_\varphi = \frac{\varphi_\alpha \frac{d\varphi_\beta}{dt} - \varphi_\beta \frac{d\varphi_\alpha}{dt}}{\varphi_\alpha^2 + \varphi_\beta^2} = \frac{\varphi_\alpha v_\beta - \varphi_\beta v_\alpha}{\varphi_\alpha^2 + \varphi_\beta^2} \quad (13)$$

The average value of (13) delivers the frequency of the vector (11), by using a low-pass filter with a cut-off frequency chosen such that to obtain the desired dynamics. The main advantages of this method are robust and less sensitive to disturbances.

Another SV method is based on the fact that the $\alpha\beta$ components of the grid voltage are mutually dependent. It is formulated as follows [39]:

$$\begin{cases} X[n+1] = \gamma R(\omega_0 T_s) X[n] + BU[n] \\ Y[n] = \gamma R(\omega_0 T_s) X[n] + DU[n] \end{cases} \quad (14)$$

where $U[n] = [v_\alpha[n], v_\beta[n]]^T$, $B = D = (1-\gamma)I_2$ in which I_2 is the 2×2 identity matrix, and $\gamma \in (0,1)$ is called the forgetting factor. A closer value of γ to one provides better filtering of the inputs, and therefore, results in less distortion in the estimated phase angle. Space vector method can be tuned to provide highly distortion-free estimation. The main drawbacks of this method are sensitivity to the input frequency variations and imbalance.

The last one presented in this paper is weighted least-squares estimation method (WLSE), which employs the recursive weighted least-squares estimation (WLSE) algorithm [40]. This method rejects the impact of negative-sequence and accommodates variations in the frequency. In addition to the threshold and change detection problems, it exhibits other shortcomings such as long transient time intervals in detecting frequency changes and computational problems associated with the LS methods.

Comparison and Selection

It could be difficult to choose a suitable one from so many PLL and synchronization schemes. The answer depends strongly on the specific requirements and applications. Generally speaking, for single-phase applications, the basic requirement is that the amplitude, phase and frequency of the input signal should be estimated precisely even under disturbances such as distortions and notches. For three-phase applications, there are further requirements such as estimations of the fundamental positive or negative sequences, whose typical applications are the flexible power control of grid-interfaced converters for distributed power generation [41] and active power filters [42] under the distorted and unbalanced conditions.

To facilitate the choice for a given requirement, Table I gives brief guidelines for the proper selection of PLL and synchronization schemes for specific applications. Note that, with the symmetrical components method, most single-phase PLL can be extended to extract the fundamental positive or negative sequences component in three-phase systems theoretically [43], but some research articles did not give the corresponding results or verifications. Therefore, “T” stands for the meaning of “theoretical feasibility” in this case.

It must be pointed out that it is only a basic preliminary guide for selection. More detailed information may be found in references.

Conclusion

A comprehensive review of phase locked loop techniques has been carried out to explore a broad perspective on their different features and applications. It is expected to provide an easy selection guidance of an appropriate PLL for specific applications.

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Table I. Selection guidance for specific applications

	Design Simplicity	Frequency adaptive & range	Distortion insensitivity	Unbalance insensitivity	Single-phase utilization
SF-PLL	Good	Average	Average	Poor	
PQ-PLL	Average	Average	Average	Poor	
DSF-PLL	Average	Average	Good	Good	
SSI-PLL	Average	Average	Good	Good	Good
DSOGI-PLL	Average	Average	Good	Good	Good
EPLL	Average	Average	Good	Good	Good
3MPLL	Average	Average	Good	Good	
Q-PLL	Average	Average	Good	T	Good
RPLL	Average	Average	Good	T	Good
PPLL	Average	Good	Good	Good	Good
ALC-PLL	Average	Average	Good	T	Good
MR-PLL	Average	Average	Good	T	Good
APLL	Average	Average	Good	Good	Good
ZCD	Good	Poor	Poor	Poor	Good
SV	Average	Poor	Average	Poor	
WLSE	Average	Average	Good	Good	

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