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# Hardware-in-the-Loop FPGA-based Simulations of Switch-mode Converters for Research and Educational Purposes

***Abstract.*** *The paper presents in details a method and results of Hardware-in-the-Loop real-time simulation of switch-mode converters in FPGA-based hardware. A mathematical description of DC-DC boost converter model, its FPGA-based implementation and debugging results are presented. The results are compared with Simulink model and practical converter. The presented method of simulation can be used for verification of discrete control in designed converters and also as an educational platform.*

***Streszczenie.*** *W artykule przedstawiono w szczegółach metodę i rezultaty symulacji przekształtników impulsowych zrealizowane w układach FPGA. Przedstawiono opis matematyczny modelu przekształtnika DC-DC podnoszącego napięcie, jego implementację w układzie FPGA oraz wyniki. Wyniki z modelu są porównywane z modelem zbudowanym w pakiecie Simulink oraz z praktyczną realizacją układu. Zaprezentowana metoda symulacji może zostać zastosowana do weryfikacji sterowania dyskretnego w projektowanych przekształtnikach oraz jako platforma edukacyjna. (**Symulacje czasu rzeczywistego przekształtników impulsowych, zrealizowane w układach FPGA, dla celów badawczych i edukacyjnych**).*

**Keywords:** Hardware-In-Loop simulation, FPGA, Real-time model, DC-DC boost converter
**Słowa kluczowe:** FPGA, czas rzeczywisty, przekształtnik DC-DC typu boost, symulacje

## Introduction

Simulation tools are commonly used for research and educational purposes in power electronics. Usually PC-based methods are used to verify operation of a system and control design. However, a controller circuit designed in PC-based simulation tools is far away from its practical implementation in a hardware. If the control system is dedicated to digital implementation (e.g. in DSP processor or FPGA) it can be verified using FPGA-based method of physical system modeling. In such method a discrete model of the power system (e.g. power electronic converter) is implemented in a FPGA IC and the controller is verified in a real time. The model of controlled system is composed of switching components, passive components and sources.

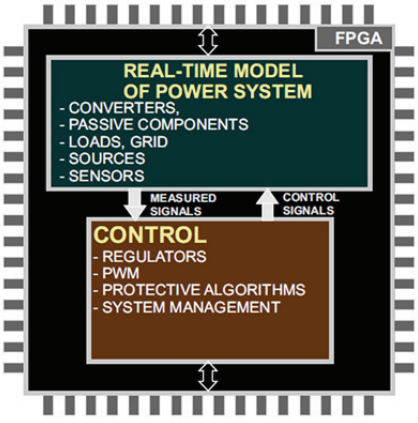


Fig. 1. Power system model implementation the in FPGA and the verification of digital control

Such method of FPGA-based implementation of model of physical components for simulation or hardware-in-loop control is used in electrical photovoltaic systems [1]-[7], power electronic converters [8]-[10] and drive systems [11]-[28]. It can be also used as an educational tool in courses of digital control.

Signals generated by the model of the system implemented in the FPGA IC can be easily analyzed in the FPGA (e.g. SignalTap II Logic Analyzer in Quartus II Software). Presenting the FPGA-based model signals by D/A (Digital-to-Analog) converters on standard oscilloscope gives the possibility of using, in evaluation of the modeled system, specific math functions (e.g. THD, FFT or PF calculation) provided by the digital oscilloscopes (Fig. 2). Thus, it is advantageously to apply such method together with FPGA's debugging tools.

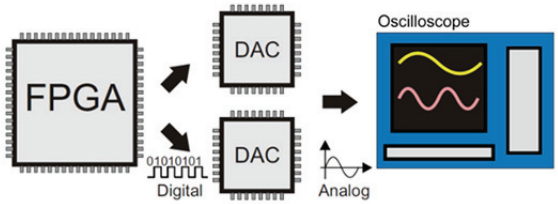


Fig. 2. Method of presentation of FPGA-based model signals from the power system implemented in the FPGA IC

A DC-DC switch-mode boost converter is one of the most commonly used converter in many applications of power electronics, such as photovoltaic systems. Presentation of its FPGA-based model is a good example of hardware simulation implementation. This paper focuses on the presentation of mathematical coding description of the DC-DC boost converter for the Hardware-in-the-Loop FPGA-based simulations and comparison with a laboratory setup. Parameters (inductance, capacitance, switching frequency etc.) of the created Matlab-Simulik and FPGA-based models were set on the basis of the laboratory converter.

## Discrete Model of Switch-Mode DC-DC Boost Converter

Fig. 3 presents a modeled topology of DC-DC boost converter.

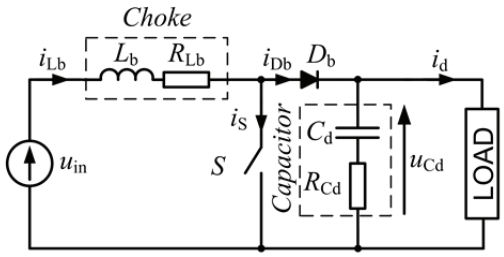


Fig. 3. DC-DC boost converter topology

Discrete-time real time model of the converter is obtained with the use of numerical methods. Numerical methods, such as Euler method does not give exact solution of differential equations but enables to estimate its

value at given point of time. Using fast enough hardware, a real-time calculations with the use of numerical methods can be realized.

The boost converter, depending on a switch state, can be divided into subcircuits presented in Fig. 4. In the Continues Current Mode (CCM) converter is described by subcircuits (a),(b), whereas during Discontinues Current Mode (DCM) converter is described by subcircuits (a),(b),(c). Each subcircuit can be described by first or second order differential equations.

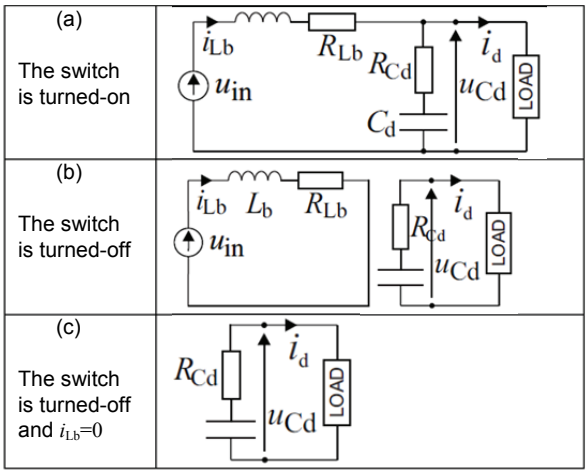


Fig. 4. DC-DC boost subcircuits analysis

For subcircuit composed of $u_{in}$, $L_b$, $R_{Lb}$, (Fig. 4b) application of Euler method for the current calculation provides following numerical algorithm:

$$(1)\quad \Delta i_{Lb} = i_{Lb}(n+1) - i_{Lb}(n) = T_p\left(\frac{1}{L_b}u_{in}(n) - \frac{R_{Lb}}{L_b}i_{Lb}(n)\right)$$

$$(2)\quad i_{Lb}(n+1) = i_{Lb}(n) + \frac{T_p}{L_b}u_{in}(n) - T_p\frac{R_{Lb}}{L_b}i_{Lb}(n)$$

$$(3)\quad i_{Lb}(n+1) = \frac{T_p}{L_b}u_{in}(n) + \left(1 - T_p\frac{R_{Lb}}{L_b}\right)i_{Lb}(n)$$

The output circuit composed of $C_d$, $R_{Cd}$ and LOAD (Fig. 4c) can be solved on the basis of the following equation (having the load current $i_d$ previously calculated):

$$(4)\quad u_{Cd} = -i_d R_{Cd} - \left(\frac{1}{C_d}\int i_d dt + u_{Cd}(0)\right)$$

$$(5)\quad \frac{du_{Cd}}{dt} = -\frac{di_d}{dt}R_{Cd} - \frac{1}{C_d}i_d$$

After discretization:

$$(6)\quad u_{Cd}(n+1) = u_{Cd}(n) - R_{Cd}i_d(n+1) + R_{Cd}i_d(n) - \frac{T_p}{C_d}i_d(n)$$

As the switch is in off-state and $i_{Lb}>0$ a second order circuit (composed of $R_{Lb}$, $L_b$, $R_{Cd}$, $C_d$ and $u_{in}$) arise in the converter (Fig. 4a). The calculation model is more complex, because $i_{Lb}$ is forced by sum of voltages ($u_{in}$-$u_{Cd}$) and the output capacitor conducts a sum of currents $i_{Lb}$-$i_d$. The numerical calculation schemes for every states of the DC-DC boost converter operation are presented in Fig. 5.

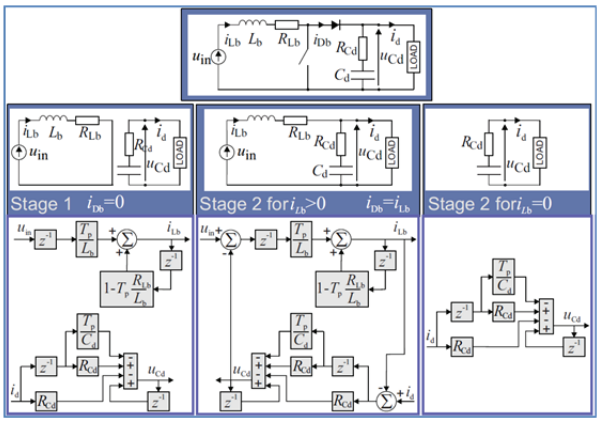


Fig. 5. The boost converter numerical solution for ideal semiconductor switches

**Control algorithm and converter parameters**

Standard control strategy of DC-DC boost converter is presented in Fig. 6. In this control strategy DC-DC boost converter stabilizes the voltage at its load.

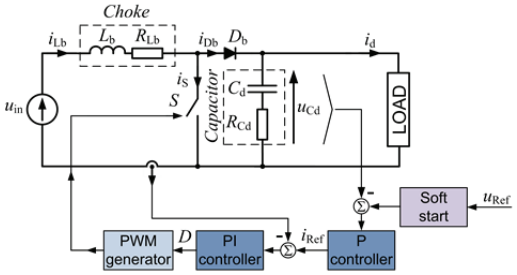


Fig. 6. DC-DC boost converter topology with standard control strategy

**Comparison between FPGA and Matlab\Simulink model**

To evaluate DC-DC boost converter FPGA-based model accuracy, comparison between Matlab\Simulink and FPGA-based model was preformed. In both simulation environments, the same DC-DC boost converter topologies were modeled and the same standard control strategies were implemented (Fig. 6). Power circuit was configured as follows: $L_b$ = 517 [µH], $R_{Lb}$ = 40 [mΩ], $C_d$ = 48,3 [uF], $R_{Cd}$ = 50 [mΩ], $f_{sw\_boost}$ = 32 [kHz], $u_{in}$ = 200 [V], $u_{ref}$ = 400 [V] and resistive load $R_{LOAD}$ = 118 [Ω].

First comparisons with Matlab-Simulink model were made to verify only the FPGA-based DC-DC boost model accuracy, without the additional uncertainty introduced by simulated control circuit. Signal driving S switch was constant and set for duty cycle 50%. Fig. 7 and Fig. 8 presents DC-DC boost converter FPGA model's voltage and currents with comparison to Matlab-Simulink model.

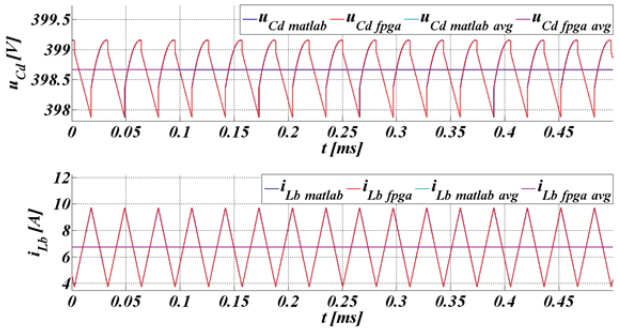


Fig. 7. Simulation waveforms of steady state (PWM duty cycle equals 50%) obtained in Matlab\Simulink and real-time FPGA model: output voltage $u_{Cd}$ and boost converter's choke current $i_{Lb}$.

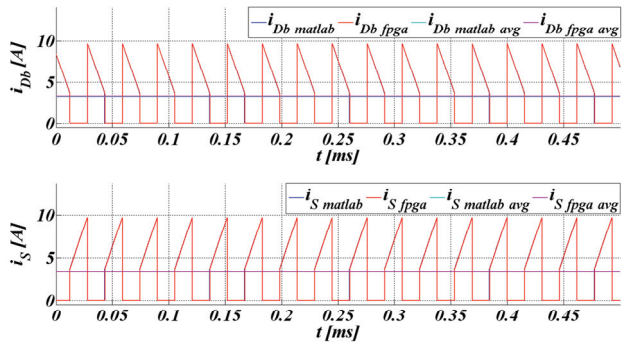


Fig. 8. Simulation waveforms of steady state (PWM duty cycle equals 50%) obtained in Matlab\Simulink and real-time FPGA model: boost converter's diode and switch currents, $i_{Db}$ and $i_S$ respectively.

On the basis of voltage and currents average values ($u_{Cd\ fpga\ avg}$, $i_{Lb\ fpga\ avg}$, $i_{Db\ fpga\ avg}$ and $i_{S\ fpga\ avg}$) in the steady state, the relative errors of FPGA-based model (without the control circuit simulation) were calculated and presented in Fig. 9. The Matlab waveforms ($u_{Cd\ matlab\ avg}$, $i_{Lb\ matlab\ avg}$, $i_{Db\ matlab\ avg}$ and $i_{S\ matlab\ avg}$) were used as reference. The mean relative errors of each presented signals are as follows: $u_{Cderr}$ = 0.001%, $i_{Dberr}$ = 0.75%, $i_{Lberr}$= 0.19%, $i_{Serr}$ = 0.63%.

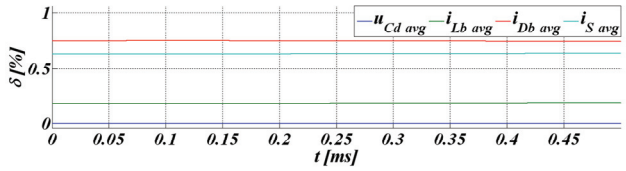


Fig. 9. Relative error of real-time FPGA model without control circuit in reference to the Matlab\Simulink results obtained during the simulation of steady state.

In advanced comparisons, DC-DC boost converter model and model of control circuits were used. Simulated system was tested in dynamic and steady state as well, to obtain the accurate comparison results. Therefore, the DC-DC boost converter soft-start method was simulated - reference output voltage $u_{Cdref}$ was raised from 200 [V] to 400 [V] with ramp 11,5 [V/ms] (Fig. 10). Four signal waveforms were compared: output voltage $u_{Cd}$, choke $L_b$, diode $D_b$ and switch $S$ currents – $i_{Lb}$, $i_{Db}$ and $i_S$ respectively. Besides the instantaneous signal values the average values were calculated and are presented in Fig. 10 - Fig. 13. Duration of averaging window lasts 10 switching periods and is equal to 312,5 [μs].

As can be seen in Fig. 10 and Fig. 12 the dynamic responses of DC-DC boost converter FPGA model's voltage and currents are highly similar to the reference ones generated by the Matlab\Simulink model.

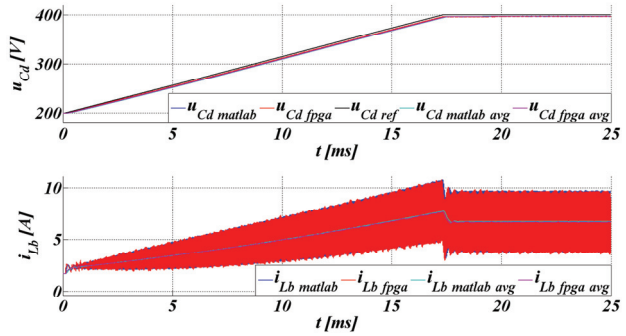


Fig. 10. Soft-start simulation waveforms of Matlab\Simulink and real-time FPGA model: output voltage $u_{Cd}$ and boost converter's choke current $i_{Lb}$.

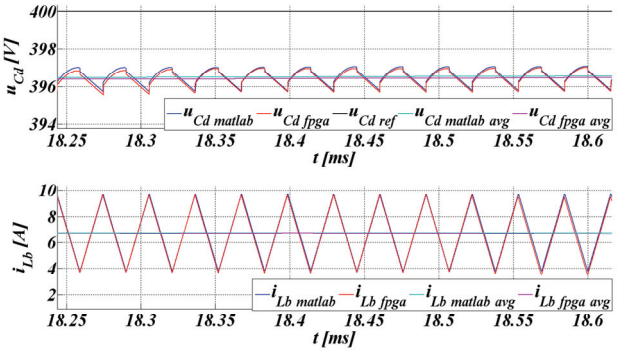


Fig. 11. Steady state simulation waveforms of Matlab\Simulink and real-time FPGA model: output voltage $u_{Cd}$ and boost converter's choke current $i_{Lb}$.

Detailed waveforms are presented in Fig. 11 and Fig. 13 which depicted the steady state moment just after the soft-start period. The instantaneous values are almost the same but small discrepancies can be observed. The probable reasons which have an effect on this difference and the accuracy of FPGA model are as follows:

- calculation of DC-DC boost converter's model are made as fixed point,
- the 12-bit control and 18-bit model signals are used which cause the visible quantization and constraint the resolution of all result values,
- the hardware clock signal is used in real-time simulations which has finite accuracy and as all electronic devices is sensitive for environmental operation conditions e.g. temperature.

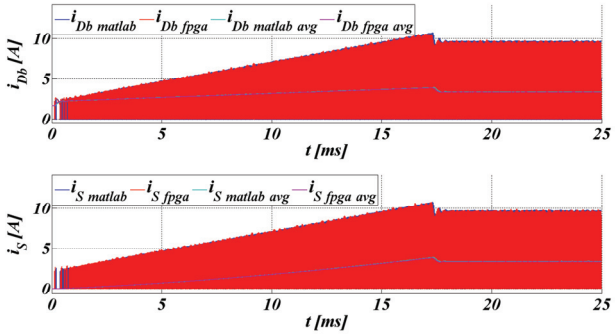


Fig. 12. Soft-start simulation waveforms of Matlab\Simulink and real-time FPGA model: boost converter's diode and switch current, $i_{Db}$ and $i_S$ respectively.

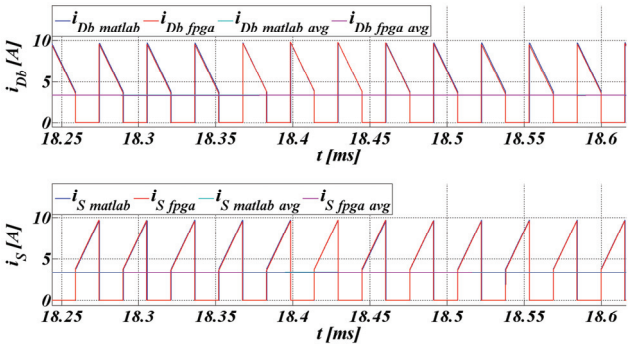


Fig. 13. Steady state simulation waveforms of Matlab\Simulink and real-time FPGA model: boost converter's diode and switch current, $i_{Db}$ and $i_S$ respectively.

On the basis of voltage and currents average values ($u_{Cd\ fpga\ avg}$, $i_{Lb\ fpga\ avg}$, $i_{Db\ fpga\ avg}$ and $i_{S\ fpga\ avg}$) the relative errors of FPGA-based model (with the control circuit simulation) were calculated and presented in Fig. 14. The Matlab waveforms

($u_{Cd\ matlab\ avg}$, $i_{Lb\ matlab\ avg}$, $i_{Db\ matlab\ avg}$ and $i_{S\ matlab\ avg}$) were used as reference. The mean relative errors of each presented signals are as follows: $u_{Cderr}$ = 0.15%, $i_{Dberr}$ = 0.76%, $i_{Lberr}$= 0.84%, $i_{Serr}$ = 1.03%.

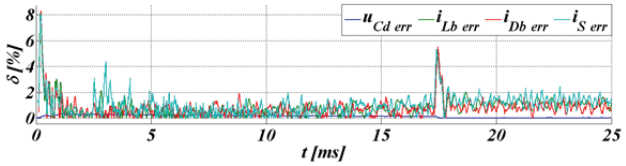


Fig. 14. Relative error of real-time FPGA model with control circuit in reference to the Matlab\Simulink results obtained during the soft-start simulation.

Main errors in simulated system are introduced not by FPGA-based model (18-bit resolution), but by FPGA-based control circuits which are simulated with 12-bit accuracy (according to typical ADC converters resolution used in control circuits of laboratory converter).

**Comparison between FPGA-based model and laboratory converter**

In order to perform verification of FPGA-based model the laboratory model of DC-DC converter was created (Fig. 15). The following parameters of DC-DC boost converter were selected: input voltage range: 200-300 [V], maximum output current 40 [A], rated DC output voltage $U_{out}$ = 400 [V], switching frequency $f_{sw\_boost}$ = 32 [kHz].

The converter employs IGBT transistor - IRGP4063 and fast, soft recovery diode DSEP30-12A. At the converter input, special 517 [μH] inductor with ferrite core was applied. On the output 47,3 [μF] capacitor bank was installed.

Analog signals are measured by Hall effect sensor (inductor current) and resistor divider (DC output voltage). Conversion of analogue signal is performed by fast 12-bit A/D converters - AD7886 with 1 [MHz] sampling frequency. All channels are sampled simultaneously.

The system control employs a FPGA controller incorporating the Cyclone II module. The FPGA is responsible for the processing of the measured signals (SPI interface), executing the control algorithm (mathematical operation: P, PI-controller, PWM modulation, etc.) and user interfacing (SignalTap II Logic Analyzer). The transistors switching sequences, generated by the control algorithm, are transmitted to the IGBT transistors via gate driver circuits (propagation delay time – 380 [ns]). Total time period necessary for all operations (signal measurement and acquisition, computation, gate driver propagation) is: $T_{conv}+T_{calc}+T_{delay}$ =1 [μs] +75 [ns] + 380 [ns] = 1,455 [μs]

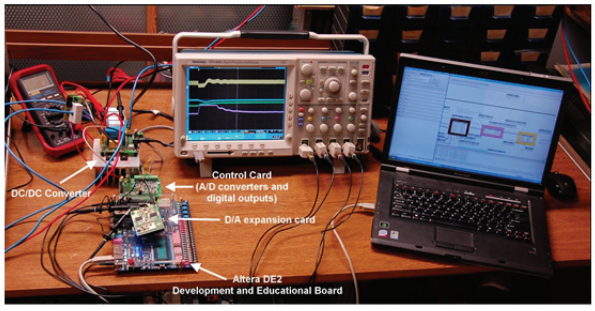


Fig. 15. Laboratory model of DC\DC converter

Control algorithm computations are triggered every analog to digital end conversion, signal transition (1 [MHz]). It is necessary to apply high resolution (min. Q20 format) in control loop (with assumption of usage 12-bit, 1 [MHz] A/D converter) in order to obtain good computation accuracy.

To ultimately verify FPGA-based DC-DC boost converter model, comparison with the practical DC-DC boost converter was performed. Model and its digital controllers were implemented in the same FPGA circuit as digital controllers of practical converter (Fig. 16). Both control circuits - FPGA model and laboratory converter, were completely the same.

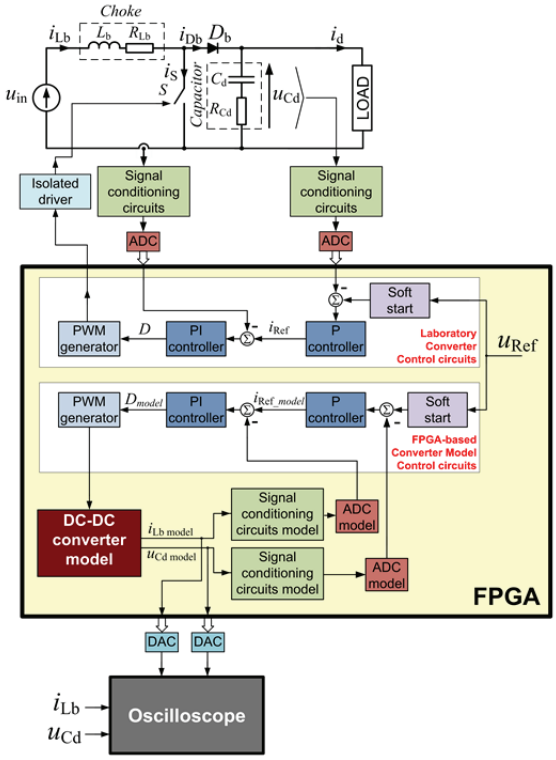


Fig. 16. Verification of FPGA-based DC-DC boost converter model as comparison with laboratory DC-DC boost converter

To accurately compare signals from FPGA-based model with practical converter, 12-bit, 1 [MHz] D/A converter extension board was used. It allows to display model signals on standard oscilloscope. Fig. 17 and Fig. 18 presents steady-state waveforms from the FPGA-based DC-DC boost converter model and laboratory DC-DC boost converter.

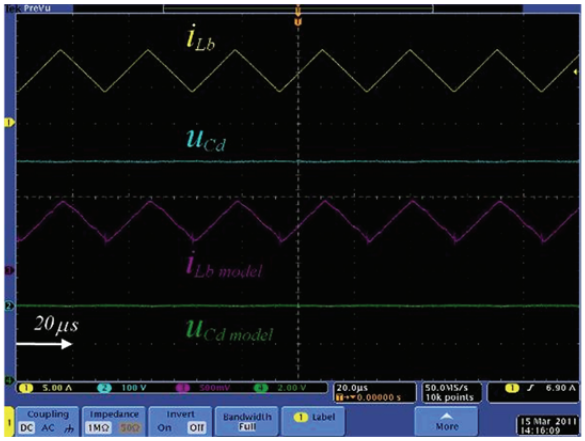


Fig. 17. Steady state waveforms, 8 samples average mode: CH1 – $i_{Lb}$ (experimental results), CH2 – $u_{Cd}$ (experimental results), CH3 – $i_{Lb\_model}$ (FPGA model results, 5 [A/div]), CH4 – $u_{Cd\_model}$ (FPGA model results, 200 [V/div])

In Fig. 18 closer examination of the FPGA-model waveforms in comparison with the practical DC-DC boost

converter waveforms is presented. Delay between FPGA-model $i_{Lb\_model}$ waveform and laboratory converter $i_{Lb}$ waveform is introduced by FPGA-model calculations and D/A converters delay time.

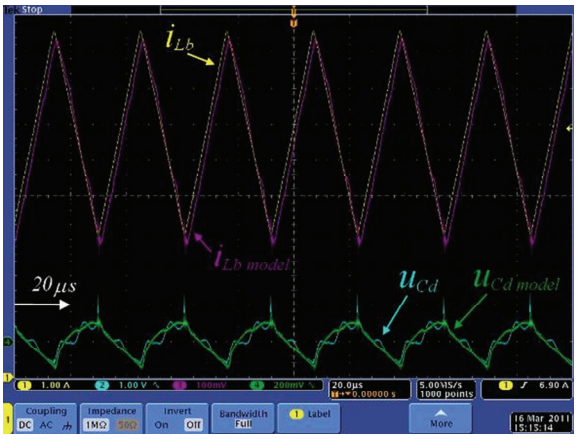


Fig. 18. Steady state waveforms, 8 samples average mode, CH1 and CH3 have the same offset level, CH2 and CH4 have the same offset level: CH1 – $i_{Lb}$ (experimental results), CH2 – $u_{Cd}$ (experimental results, AC coupling), CH3 – $i_{Lb\_model}$ (FPGA model results, 1 [A/div]), CH4 – $u_{Cd\_model}$ (FPGA model results, AC coupling, 1 [V/div])

Fig. 19 presents waveforms during the FPGA-based DC-DC boost converter model and the practical DC-DC boost converter soft-start.

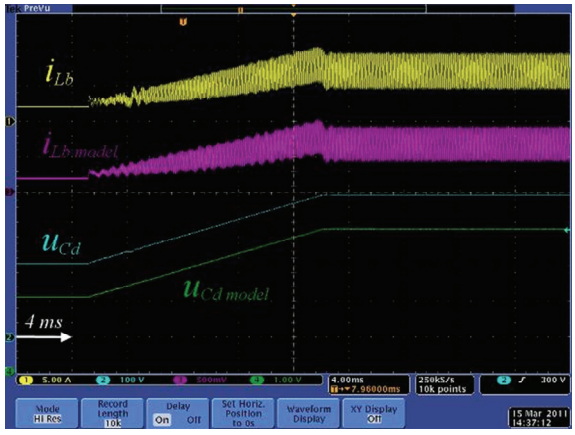


Fig. 19. Soft-start waveforms: CH1 – $i_{Lb}$ (experimental results), CH2 – $i_{Lb\_model}$ (FPGA model results, 5 [A/div]), CH3 – $u_{Cd}$ (experimental results), CH4 – $u_{Cd\_model}$ (FPGA model results, 100 [V/div])


Fig. 20. Steady state waveforms: CH1 – $i_{Lb}$ (experimental results), CH2 – $i_{Lb\ model}$ (FPGA model results, 5 [A/div]), CH3 – $i_{Db\ model}$ (FPGA model results, 5 [A/div]), CH4 – $i_{S\ model}$ (FPGA model results, 5 [A/div])

FPGA model major advantage is that all model (e.g. $i_{Lb\_model}$, $i_{Db\_model}$, $i_{S\_model}$, $u_{Cd\_model}$) and controllers signals (e.g. $I_{Ref}$, $I_{Ref\_model}$, $D$, $D_{model}$) can be visualized (Fig. 20). This possibility can be very useful in some cases of designed system evaluation.

## Research Aspects of the FPGA-Based Hardware Simulations

### *A. Real-time verification on the design stage*

Major problem in the design of controller circuits for DC-DC boost converters is DCM operation. Controller circuit have to be very robust especially during transient change of converter operating region from CCM to DCM as result of transient change of load. Real-time FPGA-based converter model can be helpful during the design stage of practical converter (especially digital controllers). Digital controller can be verified in the dedicated hardware which reduces time and costs. Fig. 21 presents waveforms during controller tests, with transient change of load from 118 [Ω] to 6,5 [kΩ].

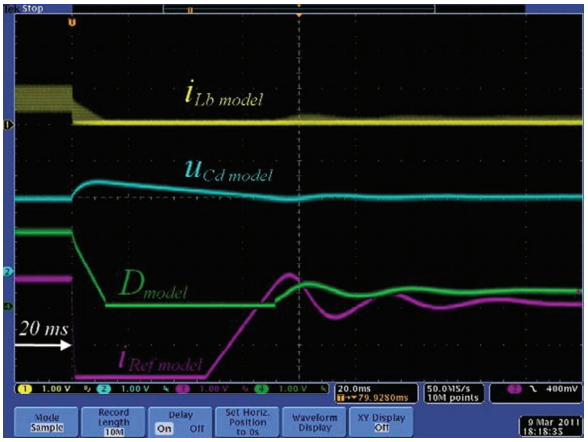


Fig. 21. Transient state waveforms, CH3 and CH4 have the same offset level: CH1 – $i_{Lb\_model}$ (FPGA model results, 10 [A/div]), CH2 – $u_{Cd\_model}$ (FPGA model results, 100 [V/div]), CH3 – $i_{Ref\_model}$ (FPGA model results, 10 [A/div]), CH4 – $D_{\_model}$ (FPGA model results, 25 [%/div])

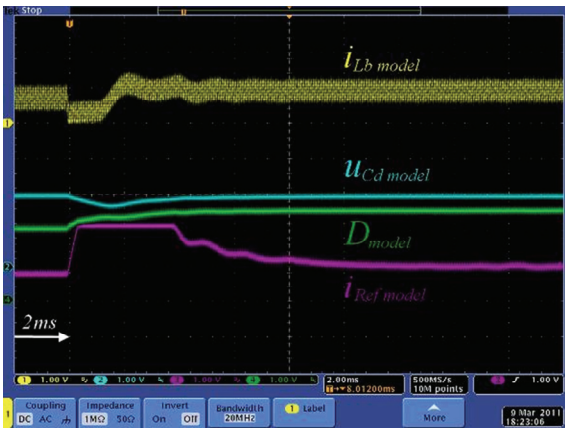


Fig. 22. Transient state waveforms, CH3 and CH4 have the same offset level: CH1 – $i_{Lb\_model}$ (FPGA model results, 10 [A/div]), CH2 – $u_{Cd\_model}$ (FPGA model results, 100 [V/div]), CH3 – $i_{Ref\_model}$ (FPGA model results, 10 [A/div]), CH4 – $D_{\_model}$ (FPGA model results, 25 [%/div])

In PV systems DC-DC boost converter topology, as first stage converter, became very popular. In this applications it is very important for the DC-DC boost controller to stabilize output voltage during transient changes of input voltage (PV array voltage). In the FPGA real time modeling, designed controller can be tested in various scenarios, even with very

rapidly changing conditions, which are sometimes very hard to be simulated practically. Fig. 22 presents waveforms during controller tests, with step change of input voltage from 150 [V] to 200 [V]. Fig. 23 presents waveforms during controller tests, with step change of input voltage from 200 [V] to 250 [V].

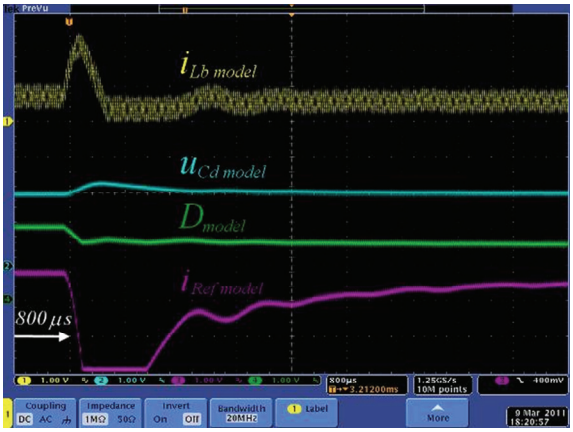


Fig. 23. Transient state waveforms, CH3 and CH4 have the same offset level: CH1 – $i_{Lb\_model}$ (FPGA model results, 10 [A/div]), CH2 – $u_{Cd\_model}$ (FPGA model results, 100 [V/div]), CH3 – $i_{Ref\_model}$ (FPGA model results, 10 [A/div]), CH4 – $D_{\_model}$ (FPGA model results, 25 [%/div])

*B. Verification of control for complex systems*

The FPGA-based simulations can be useful for verification of control of complex algorithms on dedicated hardware. Fig. 24 presents example of photovoltaic systems composed with cascaded and parallel DC-DC converters and grid connected inverter. Control design of this system, together with distributed MPPT (DMPPT) is very complex and can be tested on FPGA-based model before it practical implementation.

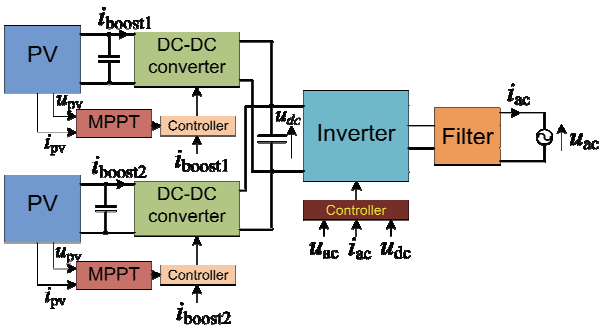


Fig. 24. Photovoltaic grid-connected system with cascaded DC sections

## Educational Aspects

FPGA-based real time models of converter can be successfully used in educational courses of power electronics and control. Debugging tools such as Signal Tap II Logic Analyzer, In System Memory Content Editor in Quartus II software or pin-based methods (e.g. with the use of D/A converters) can be very useful in this process (Fig. 25).

## Conclusions

This paper presents Hardware-in-the-Loop FPGA-based Real-time simulation of DC-DC boost converter model. The Matlab-Simulink verification as well as the Real-time comparison with laboratory converter was presented. Submitted results prove FPGA model accuracy and reliability

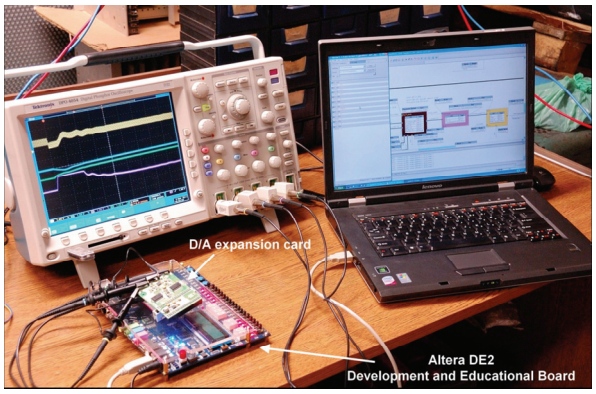


Fig. 25. FPGA-based DE2 development board and a card with D/A converters as a set for educational tools for course of digital control.

The FPGA-based Real-time modeling is a very promising method for power electronic systems evaluations, and can be successfully applied in verification of digital control for complex systems. Main advantages of this method are:

- Real-time simulations of transient states,
- Fast ability to replace model with real object (control circuit remains the same),
- Opportunity to test final control circuit during simulated emergency states without the risk of damage,

The FPGA-based Real-time modeling can also be adapted for educational courses of power electronics and control.

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