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Tolerance Maximisation in Fault Diagnosis of Analogue Electronic Circuits

***Abstract**. This paper presents method of designing periodic test excitation for fault diagnosis of analogue electronic circuits. There has been proposed maximisation of circuit components tolerances while keeping assumed level of fault diagnosis. There has also been shown that combination of fault detection and location in a single step can remarkably shorten testing time. The optimisation process involves genetic algorithm.*

***Streszczenie.** W pracy przedstawiono projektowanie periodycznego pobudzenia testowego dla diagnostyki uszkodzeń analogowych układów elektronicznych. Zaproponowano sposób maksymalizacji tolerancji elementów obwodu przy zachowaniu założonego poziomu diagnostyki uszkodzeń. Wykazano również, że połączenie etapów detekcji i lokalizacji uszkodzeń może znacząco skrócić czas testowania. (**Maksymalizacja tolerancji w diagnostyce uszkodzeń analogowych układów elektronicznych**).*

Keywords: fault diagnosis, analogue electronics, test time reduction, components tolerance, genetic algorithm.
Słowa kluczowe: diagnostyka uszkodzeń, elektronika analogowa, redukcja czasu testowania, tolerancja elementów, algorytm genetyczny.

Introduction

The test engineer must reconcile many contradictories: efficiency of fault diagnosis (how many faults can be successfully diagnosed?), access to circuit internal nodes (usually limited and expensive), circuit cost (maximise tolerances in limits defined by design, minimise circuit overhead caused by design-for-testability), test cost (strongly related with test time: single or many measurements? how much accuracy?). The test cost is a significant part of a final device cost (30% – 50% [17]). All these factors can be summarized as an optimisation problem of many related test and circuit parameters.

Two major problems of fault diagnosis of modern analogue electronic circuits (AEC) are *tolerance of components* and *limited access to internal circuit nodes*. The first causes spread of measured quantities thus resulting in *fault masking* (ambiguity sets). Lowering tolerances increases diagnosis efficiency together with device manufacturing cost. Limited access to circuit internal nodes limits sources of information about its state and possible faults.

The basic division of AEC testing is:

- *functional test*: verifies if circuit behaviour conforms the design,
- *fault diagnosis*: analysis of possible faults that may not influence circuit behaviour.

There can be distinguished three goals of AEC fault diagnosis (fig.1) [1, 14, 16, 18]:

- *fault detection*: differentiates only healthy circuits (*Go*) from faulty ones (*No Go*),
- *fault location*: locates damaged element,
- *fault identification*: determines value or at least shift below or above tolerance margin of a damaged element.

The classical sequence of a full diagnostic procedure is shown on fig. 1: detection → location → identification [1, 14, 16, 18]. Fault detection is the simplest and shortest diagnosis. It is usually performed on production line. Fault location and identification are used mostly in stage of prototyping and centring. Such multi-step analysis has advantages:

- simplification of individual steps design: fault location not need to consider healthy circuit (denoted F_0), because it is run only after detection returns *No Go* decision (fig.1),
- different optimisation goals of a separated steps (time, yield, trust level etc.).

Another division of fault diagnosis methods can be based on types of signals used for excitation of circuit under test (CUT) (fig.2):

- *DC* – the simplest and fastest, however limited by energy-storage elements. Test equipment is simple and cheap,
- *AC* analysis overcomes abovementioned. Requires relatively simple test equipment. Disadvantage is longer testing time [11, 12, 13],
- *aperiodic signals and/or transient CUT responses* potentially carries the most information about circuit state, but requires most complex and expensive test equipment [2, 5, 6, 7].

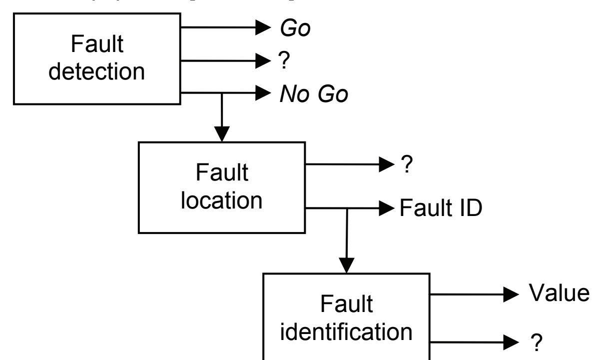

Fig.1. The main goals of fault diagnosis

The last important division of the diagnosis methods is based on moment of time when faults are simulated, fault dictionary is created and CUT responses are measured:

- *Simulate-After-Test (SAT)*: response analysis is performed after CUT measurement (*on-line*). This puts strong pressure on the analysis time shortening, because this usually dominates test time,
- *Simulate-Before-Test (SBT)*: faulty responses are simulated and stored in fault dictionary before CUT measurements (*off-line*). Total test time is determined mainly by measurement time, which is advantage over SAT methods. Disadvantage is requirement of proper prediction of possible faults and their modelling.

This paper presents solution to three selected problems:

- optimisation of input periodic (AC) excitation: for what value of its frequency there will highest efficiency of fault diagnosis?

- maximisation of components tolerance: how much the tolerances can be increased in order to keep assumed diagnosis efficiency?
- conjunction of fault detection and location in single step: does it indeed shortens total test time and what is influence on diagnosis efficiency?

There have been assumed single catastrophic faults, because such are the most common [4].

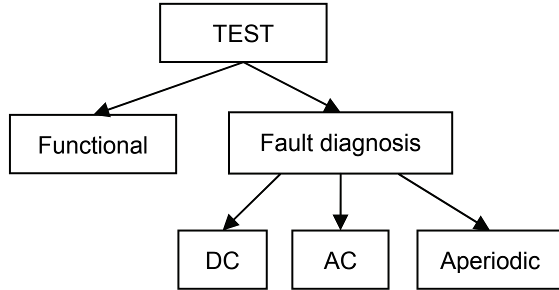

Fig.2. Division of test methods and excitations

Test methodology

The proposed method is a SBT method with fault dictionary containing border values of selected circuit responses. After CUT measurement, its response is compared to information stored in the dictionary and then appropriate decision is returned: *Go/No Go* (in case of fault detection) or fault ID (when fault location is the case). Fault identification is not taken into consideration in this paper.

There has been also proposed *full fault location*: i.e. location including state of healthy circuit (F_0). Advantage is ability to avoid location-after-detection sequence and perform both fault analyses in a single step, thus reducing test time.

Test design

A periodic (AC) signal of an amplitude A and single frequency f is applied to CUT input:

(1) $$u_{in}(t) = A\sin(2\pi ft + 0^\circ)\ [V]$$

Additional test parameters are tolerances of all discrete resistors (t_R) and capacitors (t_C) in the circuit. The Spice simulation returns four responses: root-mean square (RMS) value and phase of respectively output voltage (U_{RMS}, U_{PH}) and input current (I_{RMS}, I_{PH}). The Monte-Carlo analysis with uniform distribution is used to simulate tolerances t_R and t_C. It has been assumed that CUT is linear and amplitude A of the input excitation has such value to keep circuit working in linear region for all analysed faults. This enables taking measurements with relatively simple and cheap circuitry (even for high frequencies) and without additional post-processing (thus fast).

Example plot of U_{RMS} vs. frequency (for selected faults, specific values of t_R and t_C and circuit from fig. 6) is shown on fig. 3. Selected rectangular area on fig. 3 is zoomed on fig. 4. There are shown upper (solid line) and lower (dashed line) bounds of fault F_4 for cross section at f = 80 kHz. Dotted line corresponds to nominal value. There is also indicated distance d between neighbour fault sets F_4 and F_5. It can be observed that for a given cross section the faults F_1 and F_5 are masked (create ambiguity set F_1-F_5).

For each triple of parameters (f, t_R and t_C) and measured quantity there is set of boundary values corresponding to each fault. They delimit borders of fault sets and are used to calculate distance d_n between neighbour sets F_n and F_{n+1}:

(2) $$d_n = \begin{cases} X_{n+1}^{lower} - X_n^{upper} & if \quad X_n^{nom} < X_{n+1}^{nom} \\ X_n^{lower} - X_{n+1}^{upper} & if \quad X_n^{nom} > X_{n+1}^{nom} \\ 0 & elsewhere \end{cases}$$

where X^{upper} is upper bound, X^{lower} is lower bound and X^{nom} is nominal value of particular measured quantity (U_{RMS}, U_{PH}, I_{RMS} or I_{PH}) returned from Monte-Carlo simulation for all analysed faults ($n = 0, 1, \ldots, F_{max} - 1$).

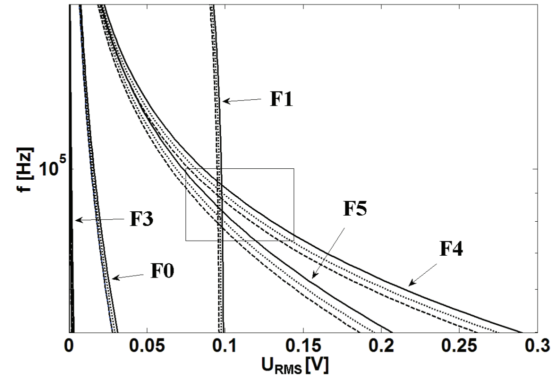

Fig.3. Example bounds of fault sets (t_R = 1%, t_C = 5%)

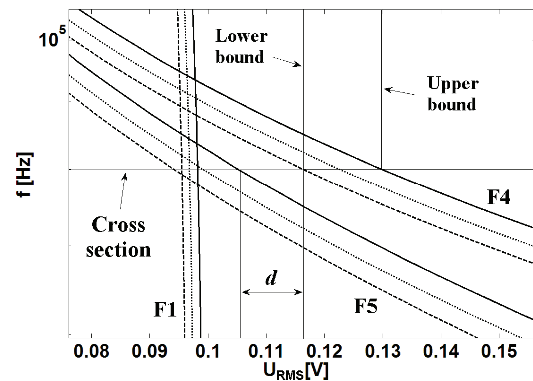

Fig.4. Zoomed area from fig. 3

If particular distance d_n is greater than assumed positive threshold distance d_{tr}:

(3) $$d_n > d_{tr}$$

such neighbour sets (and corresponding faults) are separated (distinguishable). This is used to calculate number of separated faults N, which can take values from 1 (all faults in a single ambiguity set – the worst case) to F_{max} (all faults separated – the best case), where F_{max} is number of all analysed faults:

(4) $$N \in \langle 1; F_{\max} \rangle$$

Another important quantity (DET) contains information if a set corresponding to healthy circuit (F_0) is separated ($DET = 1$) or not ($DET = 0$). Thus, if $DET = 1$it is possible to perform fault detection or full fault location (including F_0). Otherwise there can only be performed fault location and only as a second step after fault detection.

The last two calculated quantities are: minimal distance d_{min} between neighbour fault sets and sum of all neighbour distances d_{sum}:

(5) $$d_{\min} = \min(d_n) \quad n = 0,1,\ldots,F_{\max} - 1$$

(6) $$d_{sum} = \sum_{n=0}^{F_{\max}-1} d_n$$

The four abovementioned quantities (N, DET, d_{min}, d_{sum}) are used to evaluate solution of the following optimisation problem: for which values of frequency f and trying to maximise tolerances t_R and t_C, all faults (or as many as possible) are separated, F_0 is separated and d_{min} together with d_{sum} are maximised?

Genetic Algorithm

In order to solve given optimisation problem, a genetic algorithm (GA) has been used. The GA has proven to be robust and acceptably quick for problems of a multi-parameter optimisation [3, 9, 10]. However, as all of heuristic methods (except artificial annealing), there is no formal proof of its global convergence, thus no guarantee that found solution is definitely an optimal one [8].

There has been used *classic elitist GA* with schema shown on fig. 5 [8].

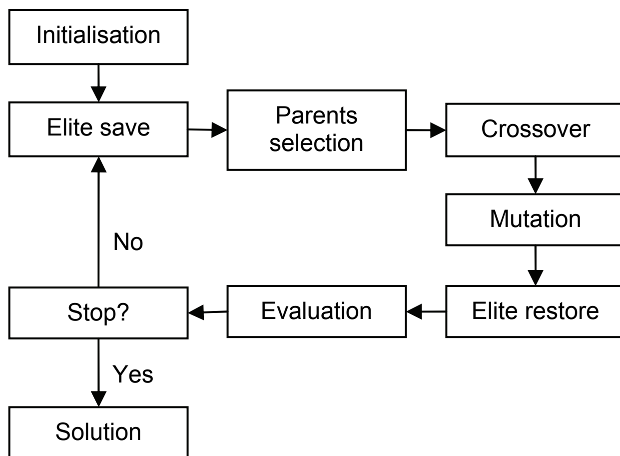

Fig.5. Schema of the genetic algorithm (an elitist model) [8]

Population size of the GA is constant. Each individual contains single linear chromosome, being a vector of genes (bits) coding specific solution: a triple f, t_R, t_C. It has been chosen Gray binary coding, because of its desired properties (e.g. lack of Hamming cliffs [8]). The number of particular bits for each triple element is a trade off between solution accuracy (bit resolution) and work time of GA (search space size).

Details of the evolution loop are following (fig.5):

- initialisation – there is not known any information *a priori* about good solution, so initial population is created randomly (uniformly): each gene takes initial value 0 or 1 with probability 0.5,
- unique elite individuals are saved which prevents the best found so far solutions from being destroyed in successive genetic operations (e.g. crossover and mutation),
- parents selection is based on binary tournament: two individuals are selected randomly (without return) from main population. The one with better (higher) value of a fitness is moved to population of parents,
- reproduction – single-point crossover is applied to parents and offspring population is created,
- succession has been realised by means of a half succession: 50% of randomly selected offspring replaces 50% of a randomly selected individuals in main (old) population. This slows down GA progress a bit, but makes it more resistant for sticking in local extremes (which is very desired feature),
- mutation – value of each gene is negated with given probability,
- elite is restored into main population (randomly chosen individuals are replaced in order to keep constant population size). Random selection does not introduce evolutionary pressure,
- the main population is evaluated: each new or modified individuals' fitness is calculated,
- stop criterion – GA stops and returns found solution after specified number of iterations.

Evaluation of an individual (coding specific solution) is the most important (and usually time consuming) step of a GA:

- chromosome is decoded into values of excitation frequency f and tolerances t_R and t_C,
- Spice simulation is performed for decoded triple (f, t_R, t_C) and all defined faults,
- quantities N, DET, d_{min} and d_{sum} are calculated,
- fitness fit is calculated (depending on measured quantity) and GA tries to maximise its value.

First step of evaluating fitness function for particular solution is normalisation of d_{min} and d_{sum}:

(9) $$d_{sum}^{norm} = \frac{d_{sum}}{d_{\max}}$$

(10) $$d_{\min}^{norm} = \frac{d_{\min}}{d_{\max}}$$

where d_{max} is maximal value of d_{sum} for particular quantity (U_{RMS}, U_{PH}, I_{RMS} or I_{PH}). This value is also used to normalise d_{min}, because:

(11) $$d_{\min} \le d_{sum}$$

Final step is calculation of fitness value for particular solution:

(12) $$fit = w_1 N + w_2 DET + w_3 t_R + w_4 t_C + \\ + w_5 d_{\min}^{norm} + w_6 d_{sum}^{norm}$$

where w_i, $i = 1, 2, \ldots, 6$ are weights used to control "importance" of particular quantity by its influence on fitness value – thus search direction of the GA.

Example

The proposed method has been verified on low-pass filter [15] (fig.6). There have been selected 12 faults $F_1 \div F_{12}$, with healthy circuit denoted F_0. Tab. 1 shows fault coding and relation to circuit elements.

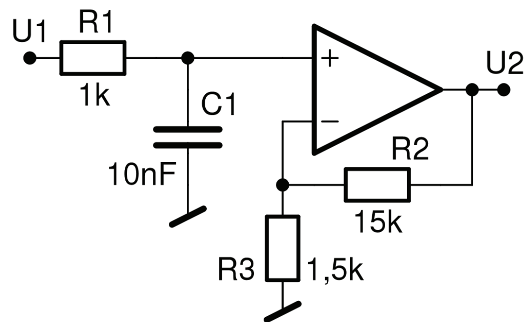

Fig.6. Low-pass filter [15]

Shorts of resistors, capacitors or selected nodes of operational amplifier have been modelled as 1 Ω resistance in parallel. Opens have been modelled as 100 MΩ

resistance in series. Operational amplifier saturation has been modelled with DC voltage source replacing amplifier output. There have been run 100 Monte–Carlo analyses for each fault (including healthy circuit).
The parameters of the GA were following:

- population size: 100 individuals,
- mutation probability (for single gene): 0.01,
- stop criterion: after 100 iterations.

Table 1. Faults codes

Fault code	Element	Fault
F_0	–	circuit healthy
F_1	R_1	short
F_2	R_1	open
F_3	R_2	short
F_4	R_2	open
F_5	R_3	short
F_6	R_3	open
F_7	C_1	short
F_8	C_1	open
F_9	Op. amp.	output saturated to +15 V
F_{10}	Op. amp.	output saturated to –15 V
F_{11}	Op. amp.	output open
F_{12}	Op. amp.	inputs short

Average calculation time of the GA was 2 min./iteration, which resulted in ca. 3.5 h total work time on a Pentium D class PC. Circuit simulation was dominating and took over 99.9 % of the iteration time. The GA has been run at least 3 times for each measured quantity: U_{RMS}, U_{PH}, I_{RMS} and I_{PH}.

Chromosome length was 26 genes (bits). 10 most significant bits x_1 have been used to code excitation frequency f in range 1 Hz ÷ 1 GHz:

$$f = 10^{ax_1}\ [Hz], \qquad a = \frac{9}{2^{10}-1} \tag{13}$$

where x_1 is decimal value of the binary number (Gray coded). Such chromosome coding gave 9 decades span of the excitation frequency f with at least 100 pts/decade resolution.

Middle 8 bits x_2 of the chromosome have coded value of resistors tolerance t_R in range 1% ÷ 90%:

$$t_R = 10^{ax_2+b}\ [\%], \qquad a = \frac{\log(90)-b}{2^8-1}, \quad b = \log 1 \tag{14}$$

8 least significant bits x_3 of the chromosome have coded value of capacitors tolerance t_C in range 5% ÷ 90%:

$$t_C = 10^{ax_3+b}\ [\%], \qquad a = \frac{\log(90)-b}{2^8-1}, \quad b = \log 5 \tag{15}$$

Such coding gave 2 decades span of the tolerances t_R and t_C with at least 100 pts/decade resolution. The minimal values of the tolerances t_R (1%) and t_C (5%) have been assumed reasonable economical limits for common consumer electronics.

The design of the optimal excitation frequency have been performed for all four measured quantities (U_{RMS}, U_{PH}, I_{RMS} and I_{PH}) separately. The same fitness function (12) has been used for each quantity with following values of the weights w_i:

$$w_1 = w_2 = 362;\ w_3 = w_4 = 2;\ w_5 = w_6 = 1 \tag{16}$$

The above weights values have been selected in order to:

- 1 percent point increase of t_R or t_C were "better" (have stronger influence on the fitness function) then maximal values of $d_{\min}^{norm}$ and d_{sum}^{norm},
- increase by 1 of the DET or N were "better" (greater) than sum of maximal values of max(t_R) = 90, max(t_C) = 90, max(d_{sum}^{norm}) = 1 and max($d_{\min}^{norm}$) = 1.

The extreme values of quantities U_{RMS}, U_{PH}, I_{RMS} and I_{PH} are presented in tab. 2:

Table 2. Border values of the quantities U_{RMS}, U_{PH}, I_{RMS} and I_{PH}

Measured quantity	Border Values	Unit
U_{RMS}	0 ÷ 1.6	[V]
U_{PH}	–200 ÷ +200	[°]
I_{RMS}	0 ÷ 10	[μA]
I_{PH}	0 ÷ 90	[°]

Maximal values of the d_{min} and d_{sum} (5,6), normalisation constant d_{max} (9,10) and threshold value d_{tr} for neighbourhood fault sets separation (3) for each quantity can be found in tab. 3:

Table 3. Maximal, normalisation and threshold values

Measured quantity	d_{sum}	d_{min}	d_{max}	d_{tr}	Unit
U_{RMS}	1.6	1.6	1.6	0.02	[V]
U_{PH}	200	200	200	5	[°]
I_{RMS}	10	10	10	0.1	[μA]
I_{PH}	90	90	90	5	[°]

The threshold values were chosen under assumption of 1% accuracy measurement, where measurement range is close to abovementioned ranges of the U_{RMS}, U_{PH}, I_{RMS} and I_{PH}.

In order to assure that tested CUT works in linear mode for all simulated faults, amplitude A of the input excitation was set to 15 mV.

The best results returned by the GA for measurements of:

- output voltage RMS value (U_{RMS}) are shown in tab. 4,
- output voltage phase (U_{PH}) are presented in tab. 5,
- input current RMS value (I_{RMS}) are placed in tab. 6,
- input current phase (I_{PH}) are in tab. 7.

Table 4. The best results for U_{RMS}

	Solution 1a	Solution 1b	Solution 1c
f [Hz]	25051.1	24056.5	23101.3
t_R [%]	7.23	5.16	5.84
t_C [%]	24.4	30.0	23.1
N	5	5	5
DET	1	1	1
d_{sum} [V]	0.33	0.33	0.41
d_{min} [V]	0.02001	0.02060	0.02055

Table 5. The best results for U_{PH}

	Solution 2a	Solution 2b	Solution 2c
f [MHz]	5.82634	2.53917	2.53917
t_R [%]	21.9	1.26	1.28
t_C [%]	65.5	42.6	43.1
N	8	10	10
DET	0	0	0
d_{sum} [°]	318	347	347
d_{min} [°]	5.06	5.05	5.01

Table 6. The best results for I_{RMS}

	Solution 3
f [MHz]	1499.52
t_R [%]	46.8
t_C [%]	90
N	4
DET	0
d_{sum} [μA]	1.41
d_{min} [μA]	0.10051

Table 7. The best results for I_{PH}

	Solution 4a	Solution 4b
f [Hz]	7895.16	7895.16
t_R [%]	2.25	1.37
t_C [%]	17.8	19.0
N	5	5
DET	0	0
d_{sum} [°]	76.3	76.1
d_{min} [°]	5.00	5.01

Fault sets and their ambiguities for found solutions are shown in tab. 8:

Table 8. Fault sets ambiguities

Solution	Fault Sets
1a, 1b, 1c	F9-F10-F2-F7-F11-F12-F3-F6, F0, F1-F8, F5, F4
2a	F2-F0, F3, F6, F1-F7, F8, F9-F10-F11, F12, F4-F5
2b, 2c	F5, F2-F0, F3, F6, F1-F7, F8, F9-F10, F11, F12, F4
3	F2-F8-F1, F0-F3-F4-F5-F6-F9-F10-F11, F12, F7
4a, 4b	F7-F2, F8, F12, F0-F3-F4-F5-F6-F9-F10-F11, F1

Conclusions

It can be observed that for given ranges of excitation frequency and circuit components tolerances:

- only measurement of U_{RMS} **enables separation of healthy circuit state** (F_0), thus fault detection,
- measurement of U_{PH} gives **the best fault location** (N = 10 of total 13 states). Unfortunately the F_0 state (healthy circuit) is not separated,
- combination of any U_{RMS} measurement and solution 2a enables **full fault location** (including F_0). This means that fault detection step can be omitted. This is possible for t_R = 5% and t_C = 30% (**low price components**),
- combination of I_{RMS} measurement and solution 2a enables **fault detection** for t_R = 22% and t_C = 65% (**very low price components**),
- the excitation frequency **does not exceed 6 MHz** and assumed measurement accuracy **does not require expensive test equipment**.

It must be noted that abovementioned combination of excitations and measurements can be easily done simultaneously (linear circuit, large difference of particular excitation frequencies) with simple, inexpensive circuits and does not introduce test time overhead.

From above observation follows that full fault coverage can be obtained without access to CUT internal nodes: the only measured quantity is output voltage and input current (generally: quantities accessible from external circuit nodes). Presented method is well suited for integrated circuits (IC).

Additionally it has been investigated that theoretically it is possible to obtain full fault location (including F_0 state) with a single measurement (any of U_{RMS}, U_{PH}, I_{RMS} or I_{PH}). Unfortunately it requires impractically low components tolerances (well below 0.1%) and high measurement accuracy (levels of ppm).

It can be agreed that the shortest test measurement (for the worst case: the lowest test frequency f = 1.5 kHz) takes **less than 1.5 ms**. This is calculated for assumption that first period of the CUT response is "wasted" for transient states to vanish. Indeed, the transient step response reaches steady state under 50 μs for all faults.

The method belongs to the SBT class of the dictionary fault diagnosis methods, so design process is *off-line* (before measurements) and its completion time (hours) is of a secondary importance. The complete test requires time of milliseconds, simple and inexpensive equipment and can be successfully conducted for CUT build from low price components.

The disadvantage is necessity of specific test design for particular circuit or device.

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