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Three-phase AC systems interfaced by current source matrix converter with Space Vector Modulation

Abstract. *The paper deals with three-phase AC systems interfaced by frequency converter without DC storage. As an interface between AC systems the current source matrix converter (CSMC) with space vector modulation is used. First the averaged state space models are formulated. Furthermore simulation and experimental test results of ca 1 kVA laboratory model are presented to confirm of the discussed circuit properties.*

Streszczenie. *W artykule przedstawiono sprzężone trójfazowe systemy prądu przemiennego z przemiennikiem częstotliwości bez magazynu energii elektrycznej typu DC. Jako sprzęg pomiędzy systemami został zastosowany przekształtnik matrycowy prądu o modulacji wektorowej. Przedstawiono model uśrednionych zmiennych stanu układu. Ponadto, w artykule przedstawiono wyniki badań symulacyjnych oraz eksperymentalnych modelu laboratoryjnego o mocy ok. 1kVA potwierdzające właściwości omawianego układu.* ***(Trójfazowe systemy prądu przemiennego sprzężone za pomocą przekształtnika matrycowego prądu o modulacji wektorowej)***

Keywords: AC/AC transmission systems; AC frequency converter; current source matrix converter.
Słowa kluczowe: system przesyłowy AC/AC, przemienniki częstotliwości, przekształtnik matrycowy prądu.

Introduction

The AC/AC frequency converters (FCs) without large DC storage elements can be treated as a competitor to the commonly used pulse width-modulated voltage-source inverter (PWM-VSI) [1]–[14]. In general, the FCs comprises direct and indirect matrix converters (MCs) [1]-[3], [9], [10], hybrid MC [11], [13] and matrix-reactance frequency converters (MRFCs) [12], [14]. For application in the industrial drive field the maximum available magnitude of the output voltage should be even a little greater than the amplitude of the input voltage. For an induction motor, a reduction of the supply voltage by 10% means 20% loss of torque capability, which cannot be accepted in most applications. Among of the FCs, the direct and indirect voltage source MCs have voltage gain lesser or equal near 1 whereas the direct current source matrix converter (CSMC) [1], [2], hybrid MCs and MRFCs have a voltage gain greater than 1. For the direct current source MC with LF transfer matrix control strategy [2], the voltage transfer ratio can be much greater than one, though voltage gain and input power factor cannot be controlled independently, but they can be controlled by properly selected control parameters.

In this paper, implementation of three-phase AC systems interfaced by the current source matrix converter (CSMC) with space vector modulation (SVM) is presented. Obtained results confirm possibility to independent control of the output voltage and input power factor of the CSMC, what is very important in FACTS or drive systems applications.

Circuit description

The schematic diagram of the analysis circuit is shown in Fig. 1. The structure and allowed switch configurations of the CSMC are similar to voltage source MC (VSMC) [1]. In discussed circuit for switch state function (1), the switch configuration constrains are expressed by (2) whereas the current and voltage relations are described by (3) and (4).

$$(1)\quad s_{jK} = \begin{cases} 1, s_{jK} \text{ on} \\ 0, s_{jK} \text{ off} \end{cases},\ j = \{a, b, c\}, K = \{A, B, C\}.$$

where: s_{jK} – state function of the switch S_{jK}.

$$(2)\quad s_{aK} + s_{bK} + s_{cK} = 1$$

$$(3)\quad \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} s_{aA} & s_{aB} & s_{aC} \\ s_{bA} & s_{bB} & s_{bC} \\ s_{cA} & s_{cB} & s_{cC} \end{bmatrix} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix} = \mathbf{T} \begin{bmatrix} i_A \\ i_B \\ i_C \end{bmatrix}$$

$$(4)\quad \begin{bmatrix} u_A \\ u_B \\ u_C \end{bmatrix} = \begin{bmatrix} s_{aA} & s_{bA} & s_{cA} \\ s_{aB} & s_{bB} & s_{cB} \\ s_{aC} & s_{bC} & s_{cC} \end{bmatrix} \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \mathbf{T}^T \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix}$$

where: $\mathbf{T}$, $\mathbf{T}$ – transform matrix and transposed transfer matrix respectively.

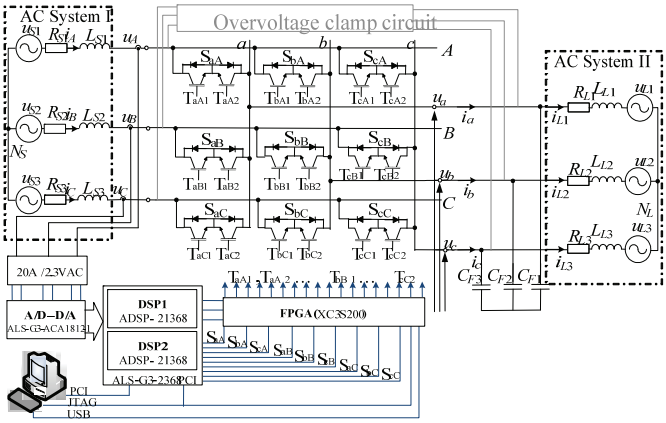

Fig. 1. AC systems interfaced by CSMC

In presented CSMC (Fig. 1) 27 configurations are allowed. From these configurations 3 zero and 18 active switch configurations are used for SVM [3]. The space vector representation of the phase output currents (5) and line to line input voltages (6) are collected in Table 1.

$$(5)\quad \underline{i}_O = \frac{2}{3}\left(i_a + \underline{a} i_b + \underline{a}^2 i_c\right) = i_O(t) e^{j\beta_O(t)},$$

$$(6)\quad \underline{u}_{IL} = \frac{2}{3}\left(u_{AB} + \underline{a} u_{BC} + \underline{a}^2 u_{CA}\right) = u_{IL}(t) e^{j\alpha_{IL}(t)}.$$

The vector representations of the $\underline{i}_O$ and $\underline{u}_{IL}$ presented in Table 1 are dual with reference to ones in circuit with VSMC [6].

Table 1. Allowed configurations of the CSMC and vector representations of the phase output currents and line to line voltages

Nr	A	B	C	$\lvert i_O \rvert$, [A]	β_O [rad]	$\lvert u_{IL} \rvert$, [V]	α_{IL} [rad]
1	a	a	a	0	-	0	-
2	b	b	b	0	-	0	-
3	c	c	c	0	-	0	-
4	a	c	c	$i_A 2/\sqrt{3}$	-π/6	$u_{ca} 2/\sqrt{3}$	5π/6
5	b	c	c	$i_A 2/\sqrt{3}$	-π/2	$u_{bc} 2/\sqrt{3}$	-π/6
6	b	a	a	$i_A 2/\sqrt{3}$	-5π/6	$u_{ab} 2/\sqrt{3}$	5π/6
7	c	a	a	$i_A 2/\sqrt{3}$	5π/6	$u_{ca} 2/\sqrt{3}$	-π/6
8	c	b	b	$i_A 2/\sqrt{3}$	π/2	$u_{bc} 2/\sqrt{3}$	5π/6
9	a	b	b	$i_A 2/\sqrt{3}$	π/6	$u_{ab} 2/\sqrt{3}$	-π/6
10	c	a	c	$i_B 2/\sqrt{3}$	-π/6	$u_{ca} 2/\sqrt{3}$	π/6
11	c	b	c	$i_B 2/\sqrt{3}$	-π/2	$u_{bc} 2/\sqrt{3}$	-5π/6
12	a	b	a	$i_B 2/\sqrt{3}$	-5π/6	$u_{ab} 2/\sqrt{3}$	π/6
13	a	c	a	$i_B 2/\sqrt{3}$	5π/6	$u_{ca} 2/\sqrt{3}$	-5π/6
14	b	c	b	$i_B 2/\sqrt{3}$	π/2	$u_{bc} 2/\sqrt{3}$	π/6
15	b	a	b	$i_B 2/\sqrt{3}$	π/6	$u_{ab} 2/\sqrt{3}$	-5π/6
16	c	c	a	$i_C 2/\sqrt{3}$	-π/6	$u_{ca} 2/\sqrt{3}$	-π/2
17	c	c	b	$i_C 2/\sqrt{3}$	-π/2	$u_{bc} 2/\sqrt{3}$	π/2
18	a	a	b	$i_C 2/\sqrt{3}$	-5π/6	$u_{ab} 2/\sqrt{3}$	-π/2
19	a	a	c	$i_C 2/\sqrt{3}$	5π/6	$u_{ca} 2/\sqrt{3}$	π/2
20	b	b	c	$i_C 2/\sqrt{3}$	π/2	$u_{bc} 2/\sqrt{3}$	-π/2
21	b	b	a	$i_C 2/\sqrt{3}$	π/6	$u_{ab} 2/\sqrt{3}$	π/2

Using averaged state space method we can obtain averaged state space equations which in general form are expressed by (7). Detailed analysis of (7) with two frequencies DQ transformation like in [15] is treated in this paper as a distinct issue.

Control and commutation strategies

The functional diagram of the control circuit is shown in Fig. 2. At the beginning the source voltage vector position is defined based upon the source current vector position. At the same time the load currents space vector i_O, with desired amplitude and frequency f_L, is set. In the next step according to Fig. 3 sector numbers S_0, S_i and the phase angels α'_0, β'_i are identify. The phase angels α'_0, β'_i are defined with respect to the bisecting line of suitable sector and limited according to (8).

Subsequently four on-time ratios according to (9)-(12) are calculated. Four active and one zero switch configurations (SC) are selected according to Table 2 and 3. The switched-on times for selected SC are calculated from (9)-(12) and expressed by (13), (14).

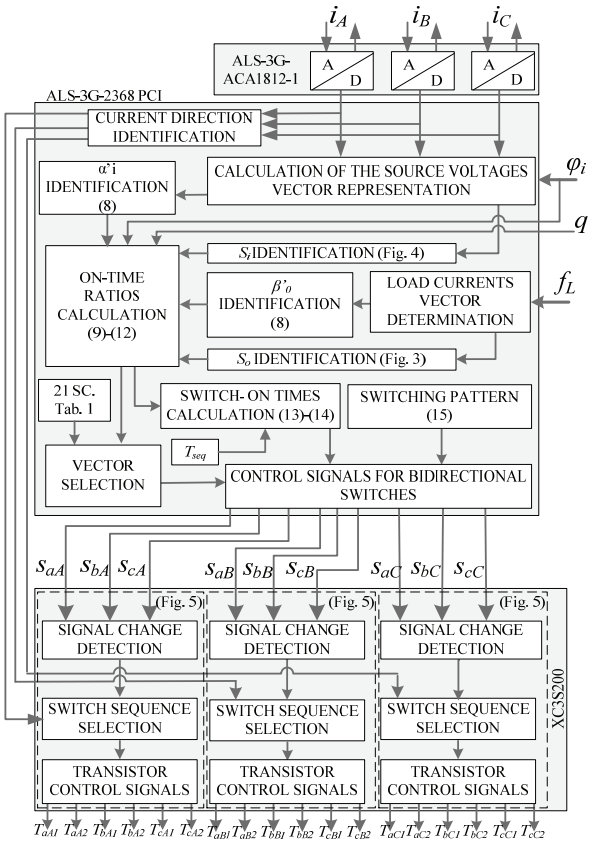

Fig. 2. Functional diagram of the control circuit

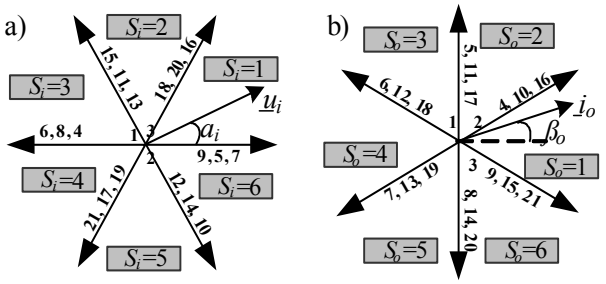

Fig. 3. Space vector representations, a) source phase voltages (u_{AN}, u_{BN}, u_{CN}), b) phase load currents

$$
\begin{bmatrix} L_{S1}d\bar{i}_A/dt \\ L_{S2}d\bar{i}_B/dt \\ L_{S3}d\bar{i}_C/dt \\ L_{L1}d\bar{i}_{L1}/dt \\ L_{L2}d\bar{i}_{L2}/dt \\ L_{L3}d\bar{i}_{L3}/dt \\ C_{L1}d\bar{u}_{L1}/dt \\ C_{L2}d\bar{u}_{L2}/dt \\ C_{L3}d\bar{u}_{L3}/dt \end{bmatrix} \cong \begin{bmatrix} -R_{LS1} & 0 & 0 & 0 & 0 & 0 & -d_{aA} & -d_{aB} & -d_{aC} \\ 0 & -R_{LS2} & 0 & 0 & 0 & 0 & -d_{bA} & -d_{bB} & -d_{bC} \\ 0 & 0 & -R_{LS3} & 0 & 0 & 0 & -d_{cA} & -d_{cB} & -d_{cC} \\ 0 & 0 & 0 & -R_{L1} & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & -R_{L2} & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & -R_{L3} & 0 & 0 & 1 \\ d_{aA} & d_{bA} & d_{cA} & -1 & 0 & 0 & 0 & 0 & 0 \\ d_{aB} & d_{bB} & d_{cB} & 0 & -1 & 0 & 0 & 0 & 0 \\ d_{aC} & d_{bC} & d_{cC} & 0 & 0 & -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \bar{i}_A \\ \bar{i}_B \\ \bar{i}_C \\ \bar{i}_{L1} \\ \bar{i}_{L2} \\ \bar{i}_{L3} \\ \bar{u}_a \\ \bar{u}_b \\ \bar{u}_c \end{bmatrix} + \begin{bmatrix} u_{S1} \\ u_{S2} \\ u_{S3} \\ -u_{L1} \\ -u_{L2} \\ -u_{L3} \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{7}
$$

where: d_{jK} – instantaneous pulse duty factor of switch control signals of the switches S_{jK} according to control strategy.

(8) $-\pi/6 < \alpha'_i < \pi/6 \quad -\pi/6 < \beta' o < \pi/6,$

(9) $$\delta_1 = (-1)^{S_O+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_i-\pi/3)\cos(\beta'_o-\pi/3)}{\cos\varphi_i},$$

(10) $$\delta_2 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_i-\pi/3)\cos(\beta'_o+\pi/3)}{\cos\varphi_i},$$

(11) $$\delta_3 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_i+\pi/3)\cos(\beta'_o-\pi/3)}{\cos\varphi_i},$$

(12) $$\delta_4 = (-1)^{S_0+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_i+\pi/3)\cos(\beta'_o+\pi/3)}{\cos\varphi_i},$$

(13) $t_1 = |\delta_1|T_{seq}, \quad t_2 = |\delta_2|T_{seq}, \quad t_3 = |\delta_3|T_{seq}, \quad t_4 = |\delta_4|T_{seq},$

(14) $t_0 = |\delta_0|T_{seq} = T_{seq} - (|\delta_1| + |\delta_2| + |\delta_3| + |\delta_4|)T_{seq}.$

Table 2. Colection of the active configurations assigned to sectors and on time ratios

$(S_i = 1\cup4) \cap (S_o=1\cup4)$	19	16	21	18	7	4	9	6
$(S_i = 2\cup5) \cap (S_o=1\cup4)$	17	20	19	16	5	8	7	4
$(S_i = 3\cup6) \cap (S_o=1\cup4)$	21	18	17	20	9	6	5	8
$(S_i = 1\cup4) \cap (S_o=2\cup5)$	13	10	15	12	19	16	21	18
$(S_i = 2\cup5) \cap (S_o=2\cup5)$	11	14	13	10	17	20	19	16
$(S_i = 3\cup6) \cap (S_o=2\cup5)$	15	12	11	14	21	18	17	20
$(S_i = 1\cup4) \cap (S_o=3\cup6)$	7	4	9	6	13	10	15	12
$(S_i = 2\cup5) \cap (S_o=3\cup6)$	5	8	7	4	11	14	13	10
$(S_i = 3\cup6) \cap (S_o=3\cup6)$	9	6	5	8	15	12	11	14
	$\delta_1>0$	$\delta_1<0$	$\delta_2>0$	$\delta_2<0$	$\delta_3>0$	$\delta_3<0$	$\delta_4>0$	$\delta_4<0$

Table 3. Collection of the zero configurations assigned to sectors and on time ratios

	$S_o = 1\cup4$		$S_o = 2\cup5$		$S_o = 3\cup6$	
$S_i = 1\cup4$	2	1	2	1	2	1
$S_i = 2\cup5$	1	3	1	3	1	3
$S_i = 3\cup6$	3	2	3	2	3	2
	$\delta_4>0$	$\delta_4<0$	$\delta_4>0$	$\delta_4<0$	$\delta_4>0$	$\delta_4<0$

Selected SC (vectors) are turned on according to the sequence described by (15), where for example δ_3 means that SC selected according to above described principles and assigned in Table 2 to δ_3 must be switched on as the first one for the time t_3. In Fig. 4 there are the geometrical interpretation examples how vector representations of the phase input voltage u_I, and the phase load current are formed. Furthermore in Fig. 4a it is shown how the control of φ_i (input power factor) is achieved by controlling of α_i.

(15) $$\delta_3 \rightarrow \delta_1 \rightarrow \delta_2 \rightarrow \delta_4 \rightarrow \delta_0$$

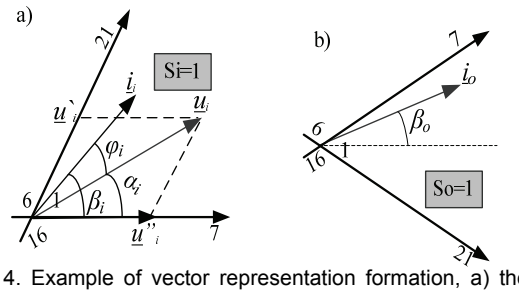

Fig. 4. Example of vector representation formation, a) the phase input voltage vector position, b) the phase output current vector position

Furthermore in control circuit of the discussed CSMC a four step commutation strategy is used (Fig. 5).

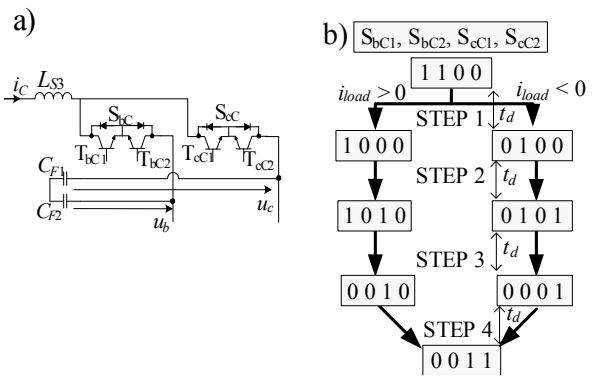

Fig. 5. Four step commutation strategy, a) simplified schematic diagram, b) commutation description; t_d – duration time of the commutation step

Simulation and experimental test results

A simulation study was carried out using the Matlab Simulink simulation package whereas operation of the discussed system with CSMC have been validated using modified laboratory model which have a 1 kVA full-load capability [14]. The electrical circuit scheme is shown in Fig. 1 whereas view of the experimental setup is shown in Fig. 6. Relevant simulation and experimental circuit parameters are collected in Table 4.

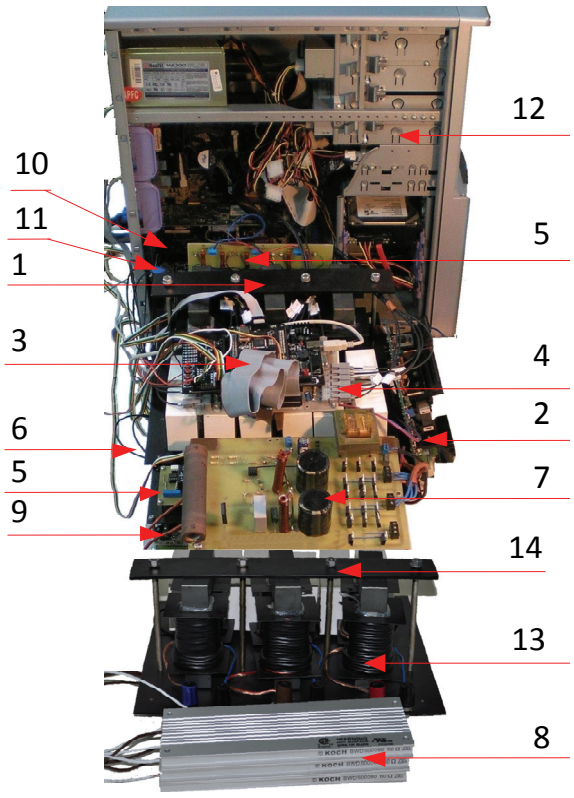

Fig. 6. Experimental setup of the laboratory model; 1 – Source inductance; 2 – AC-DC supplier; 3 – FPGA card (ZL9PLD); 4 – Optical transmitters; 5 – Input current measurement circuit; 6 – Optical receiver and gate driver circuits; 7 – Over-voltage protection circuit; 8 – Load resistors; 9 – Radiator and mine circuit transistors, 10 – DSP card (ALS-G3-2368P); 11 – AD-DA converters card (ALS-G3-ACA1812-1); 12 – PC; 13 – Output capacitances and load inductances

Table 4. Simulation and laboratory model parameters

Parameter	Symbol	Values	
		Simulation	Experiment
Source voltage/ frequency	U_S / f	230 V/50 Hz	40 V / 50 Hz
Load voltage/ frequency	U_L / f	adjustment	adjustment
Switching sequence period time	T_{seq}	0.2 ms	
Resistance	R_S; R_L	0.5 Ω	
Inductance	L_S; L_L	10 mH; 1 mH	
Capacitance	C_F	10 μF	

The simulation test results for passive load ($U_L = 0$) are shown in Fig.7. As seen, for different values of setting frequency of the load current very close unity displacement power factor (UDPF) exist for source side of the system (AC system I). The transition from lower to higher frequency at load side (AC system II) is almost without any effect on the amplitude of load voltage.

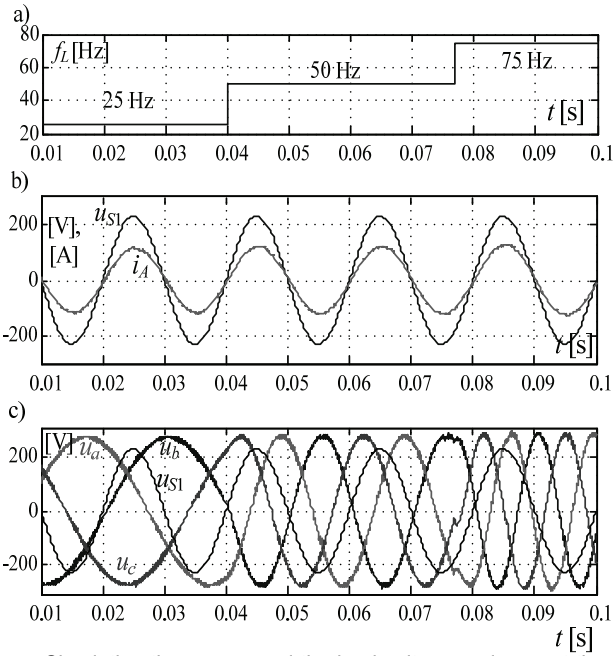

Fig. 7. Simulation the source and the load voltage and current time waveforms at different values of setting frequency of the load current, a) frequency sweep, b) the source phase voltage and current, c) the phase source and load voltage

In Fig. 8 there are example of simulation time waveforms of the voltages and currents of presented systems for different setting frequency of the load current. In this figure is also visible that phase load voltages are a little greater than supplying voltages. Investigated CSMC gives possibility to setting of the load voltage phase shifting what is shown in Fig. 9. The load voltage phase shifting influence on voltage gain (Fig. 10a) but gives favourable possibility to active power flow control what is shown in Fig. 10b. Experimental time waveforms are shown in Fig. 11 and Fig. 12. From Fig. 11 is visible that, for different values of setting frequency of the load current, very close unity displacement power factor (UDPF) is possible for source side of the system I. In Fig. 12 are shown exemplary experimental time waveforms of the source and load voltages and currents for different settings of the voltages frequency for $q = 0.866$ and unity displacement power factor. The source current is maintained sinusoidal and in phase with source voltage.

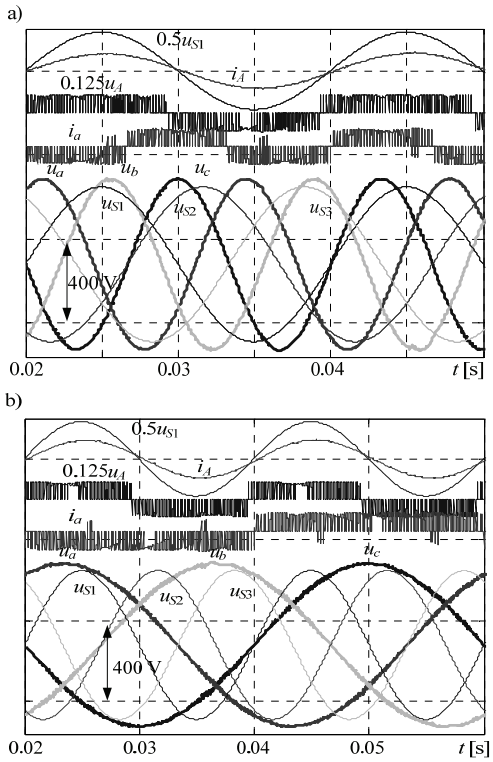

Fig. 8. Simulation voltage and current time waveforms at current gain $q = 0.8$, a) for the load frequency $f_L = 75$ Hz, b) for the load frequency $f_L = 25$ Hz

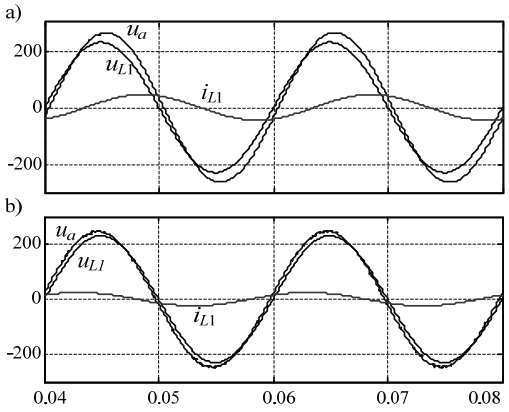

Fig. 9. Simulation phase load voltage shifting demonstration for f_L= 50 Hz, a) phase lead, b) phase lag

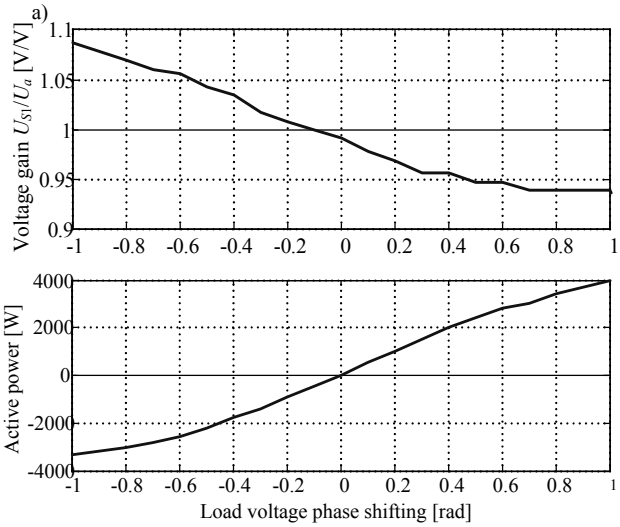

Fig. 10. Influence of the load voltage phase shifting, a) on phase voltage gain, b) on load active power

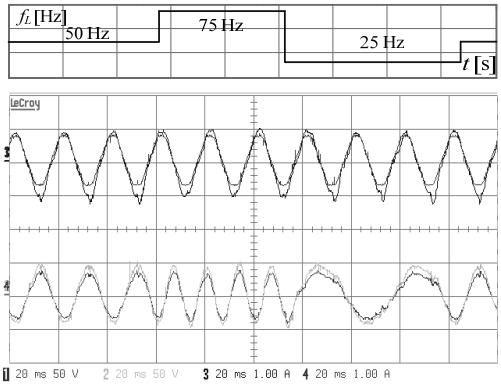

Fig. 11. Experimental source and load voltage and current time waveforms at different values of setting frequency of the load current, a) frequency sweep, b) the source phase voltage and current, c) the phase source and load voltage
1 - source phase voltage u_{S1}, 2 – load phase voltage u_a, 3 – source current i_A, 4 – load current i_{L1}

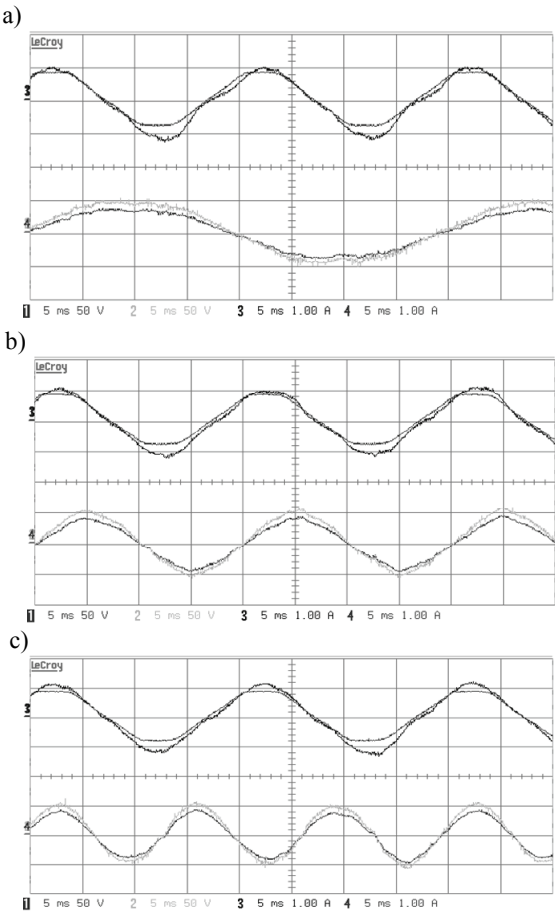

Fig. 12. Experimental voltage and current time waveforms at current gain q = 0.866, a) for the load frequency f_L = 25 Hz, b) for load frequency f_L = 50 Hz, c) for load frequency f_L = 75 Hz
1 – the source phase voltage u_{S1}, 2 – the load phase voltage u_a, 3 – the source current i_A, 4 – the load current i_{L1}

Conclusions

Implementation of three-phase AC systems interfaced by the current source matrix converter (CSMC) with space vector modulation (SVM) has been presented. In general, the simulation and experimental test results, obtained for open loop control, confirm that proposed solution can be used to control power flow between AC systems. Detailed theoretical analysis in steady and transient states and closed loop control of the presented system solution will be the subject of investigation in the near future.

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